

LAMPIRAN

LAMPIRAN

• LAMPIRAN 1

PROGRAM

```
#include <reg51.h>

sbit valve_dingin    =    P0^5;
sbit oo_valve_panas  =    P0^7;
sbit bf_valve_panas  =    P0^6;
sbit pompa           =    P0^4;

sbit egelas         =    P2^2;
sbit dgelas         =    P2^3;
sbit sgelas         =    P2^4;
sbit panas           =    P2^5;
sbit biasa           =    P2^6;
sbit dingin          =    P2^7;

#define infra                P1

int kondisi,banyak,waktu,waktus;

void delay_timer(int loop2)
{
    int aa;
    do
    {
        loop2--;
        for (aa=0;aa<=5;aa++)
        {
            TMOD=0B00010000;
            TH1=0X3C;
            TL1=0XAF;
            TR1=1;
            while (TF1==0);
            TR1=0;
            TF1=0;
        }
    }
    while (loop2!=0);
    TR1=0;
    TF1=0;
}
```

```

void main()
{
awal:

P0=0x00;

P2=0xFF;
P1=0xFF;

banyak=0;
kondisi=0;
waktu=0;
waktus=0;
oo_valve_panas=1;          //tutup valve panas
bf_valve_panas=0;          //tutup valve panas
valve_dingin=0;
pompa=1;
delay_timer(9);
oo_valve_panas=0;
P1=0x00;
delay_timer(2);
P1=0xFF;

while (banyak==0)  //-----//ukuran gelas dan isi
yang diinginkan
{

//-----// seperempat gelas
    if (egelas==0)

        {
            while (waktus==0)
            {
                if (infra==0B00011111){waktus='1';}    //gelas kecil
                if (infra==0B00001111){waktus='2';}    //gelas sedang
                if (infra==0B00000011){waktus='3';}    //gelas besar
                banyak='1';
            }
        }

//-----//setengah gelas
    if (dgelas==0)

        {
            while (waktus==0)

```

```

        {
            if (infra==0B00011111){waktus='4';} //gelas kecil
            if (infra==0B00001111){waktus='5';} //gelas sedang
            if (infra==0B00000011){waktus='6';} //gelas besar
            banyak='2';
        }
    }

//-----//satu gelas penuh
    if (sgelas==0)

    {
        while (waktus==0)
        {
            if (infra==0B00011111){waktus='7';} //gelas kecil
            if (infra==0B00001111){waktus='8';} //gelas sedang
            if (infra==0B00000011){waktus='9';} //gelas besar
            banyak='3';
        }
    }

while (kondisi==0)//-----// kondisi air yang mau dikeluarkan???
{
    //-----//Panas
    if (panas==0)
    {
        kondisi='1';
        while (waktu==0)
        {
            if (waktus=='1') {waktu=11;}//seperempat gelas kecil panas
            if (waktus=='2') {waktu=12;}//seperempat gelas sedang panas
            if (waktus=='3') {waktu=15;}//seperempat gelas besar panas (fix)
            if (waktus=='4') {waktu=22;}//setengah gelas kecil panas
            if (waktus=='5') {waktu=24;}//setengah gelas sedang panas
            if (waktus=='6') {waktu=30;}//setengah gelas besar panas
            if (waktus=='7') {waktu=44;}//segelas kecil panas
            if (waktus=='8') {waktu=48;}//segelas sedang panas
            if (waktus=='9') {waktu=60;}//segelas besar panas
        }
    }

    //-----//biasa
    if (biasa==0)
    {
        kondisi='2';
    }
}

```

```

while (waktu==0)
{
if (waktus=='1') {waktu=10;}//seperempat gelas kecil biasa
if (waktus=='2') {waktu=11;}//seperempat gelas sedang biasa
if (waktus=='3') {waktu=13;}//seperempat gelas besar biasa
if (waktus=='4') {waktu=20;}//setengah gelas kecil biasa
if (waktus=='5') {waktu=22;}//setengah gelas sedang biasa
if (waktus=='6') {waktu=26;}//setengah gelas besar biasa
if (waktus=='7') {waktu=40;}//segelas kecil biasa
if (waktus=='8') {waktu=44;}//segelas sedang biasa
if (waktus=='9') {waktu=52;}//segelas besar biasa
}
}

//-----//dingin
if (dingin==0)
{
kondisi='3';
while (waktu==0)
{
if (waktus=='1') {waktu=14;}//seperempat gelas kecil dingin
if (waktus=='2') {waktu=16;}//seperempat gelas sedang dingin
if (waktus=='3') {waktu=20;}//seperempat gelas besar dingin
if (waktus=='4') {waktu=28;}//setengah gelas kecil dingin
if (waktus=='5') {waktu=32;}//setengah gelas sedang dingin
if (waktus=='6') {waktu=40;}//setengah gelas besar dingin
if (waktus=='7') {waktu=56;}//segelas kecil dingin
if (waktus=='8') {waktu=64;}//segelas sedang dingin
if (waktus=='9') {waktu=80;}//segelas besar dingin
}
}
}

if (kondisi=='1') //kondisi air yang diminta panas: valve panas buka, valve
dingin tutup,dgn delay sesuai input gelas & isi
{
oo_valve_panas=1;
bf_valve_panas=1;
valve_dingin=0;
pompa=0;
delay_timer(waktu);
}

if (kondisi=='2') //kondisi air yang diminta biasa: valve panas buka, valve
dingin buka,dgn delay sesuai input gelas & isi
{
oo_valve_panas=1;

```

```

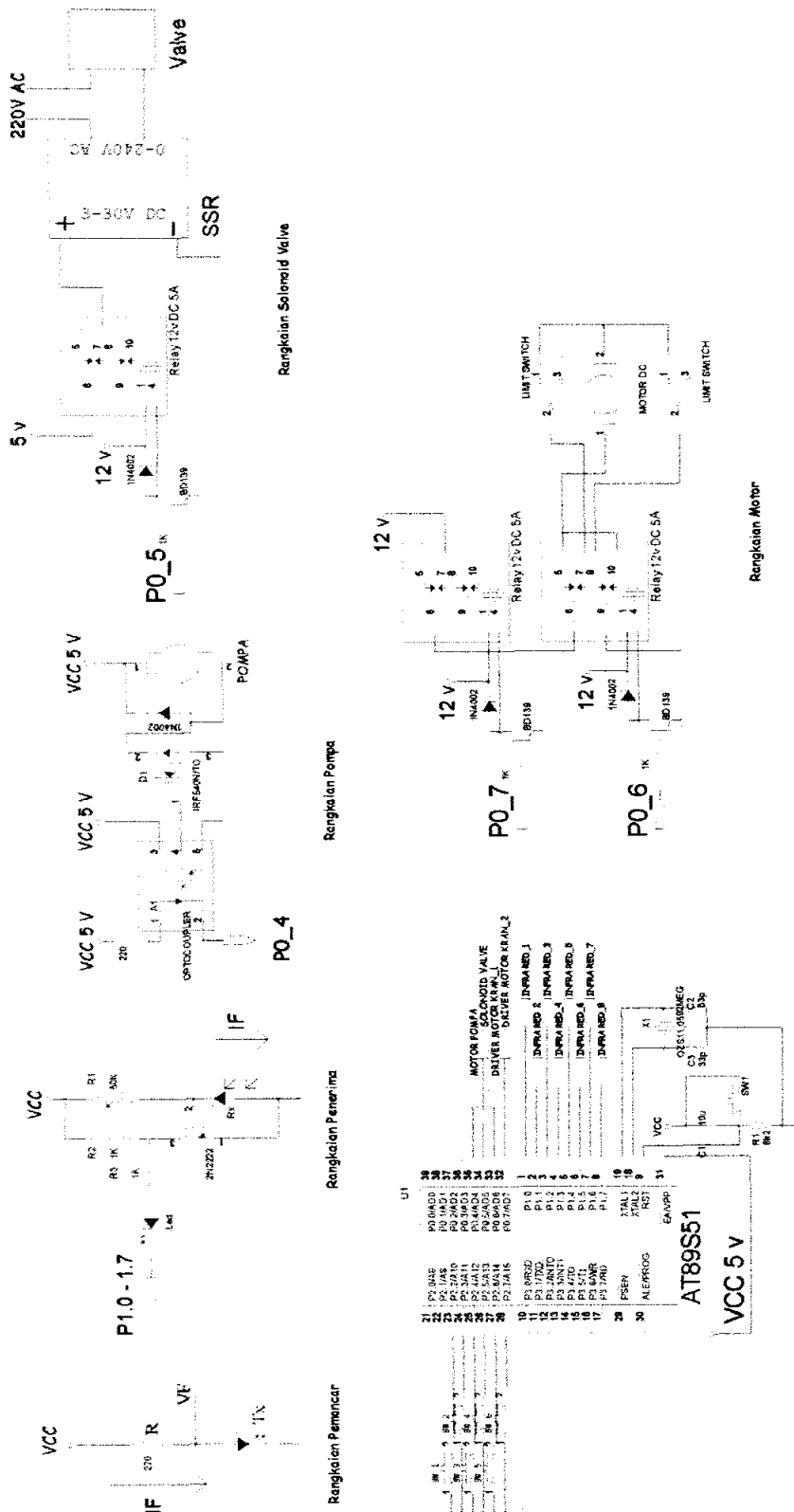
        bf_valve_panas=1;
        valve_dingin=1;
        pompa=0;
        delay_timer(waktu);
    }
    if (kondisi=='3')    //kondisi air yang diminta dingin: valve panas tutup. valve
dingin buka,dgn delay sesuai input gelas & isi
    {
        oo_valve_panas=0;
        bf_valve_panas=0;
        valve_dingin=1;
        pompa=0;
        delay_timer(waktu);
    }
    pompa=1;
    valve_dingin=0;    //tutup alve dingin
    oo_valve_panas=1;    //tutup valve panas
    bf_valve_panas=0;    //tutup valve panas

    delay_timer(20);    //delay sebelum program kembali ke awal untuk memberi
kesempatan perulangan
    goto awal;
}

```

• LAMPIRAN 2

RANGKAIAN LENGKAP



Features

- Compatible with AVR CS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
 - Endurance: 1000 Write/Erase Cycles
- 1.0V to 5.5V Operating Range
- Full-Speed Operation: 100 kHz to 33 MHz
- Two-Level Programmable Memory Lock
- 8 x 8-bit Internal SRAM
- Programmable I/O Lines
- Two 16-bit Timer/Counters
- Two Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Internal Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a cost-effective and flexible solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of SRAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five- or two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and logic circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM content but freezes the oscillator, disabling all other chip functions until the next external reset or hardware reset.



**8-bit
Microcontroller
with 4K Bytes
In-System
Programmable
Flash**

AT89S51

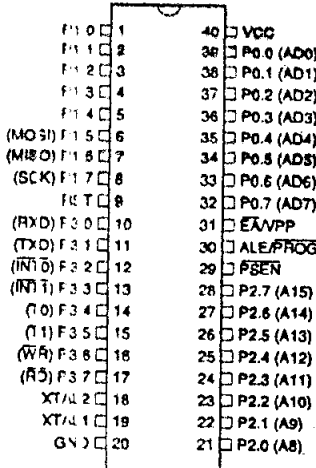
Preliminary

Rev. 2487A-10/01

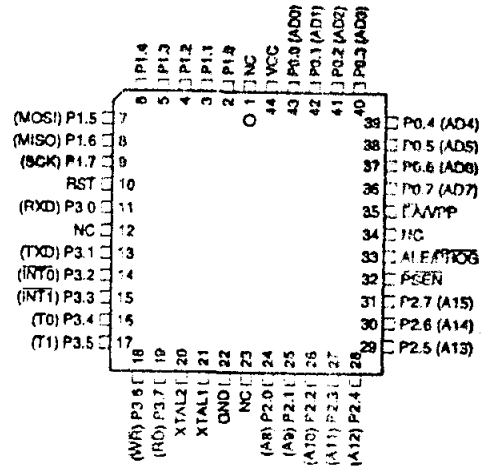


Configurations

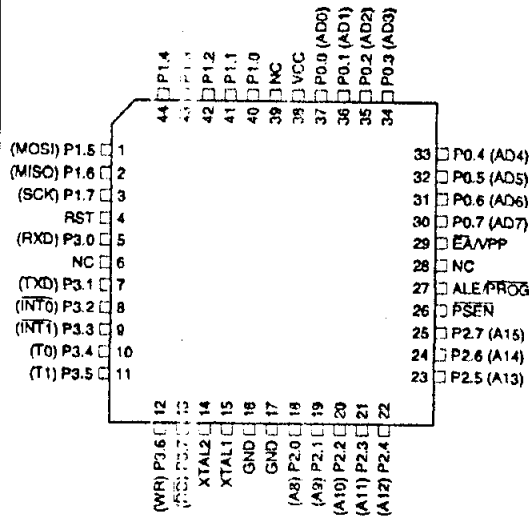
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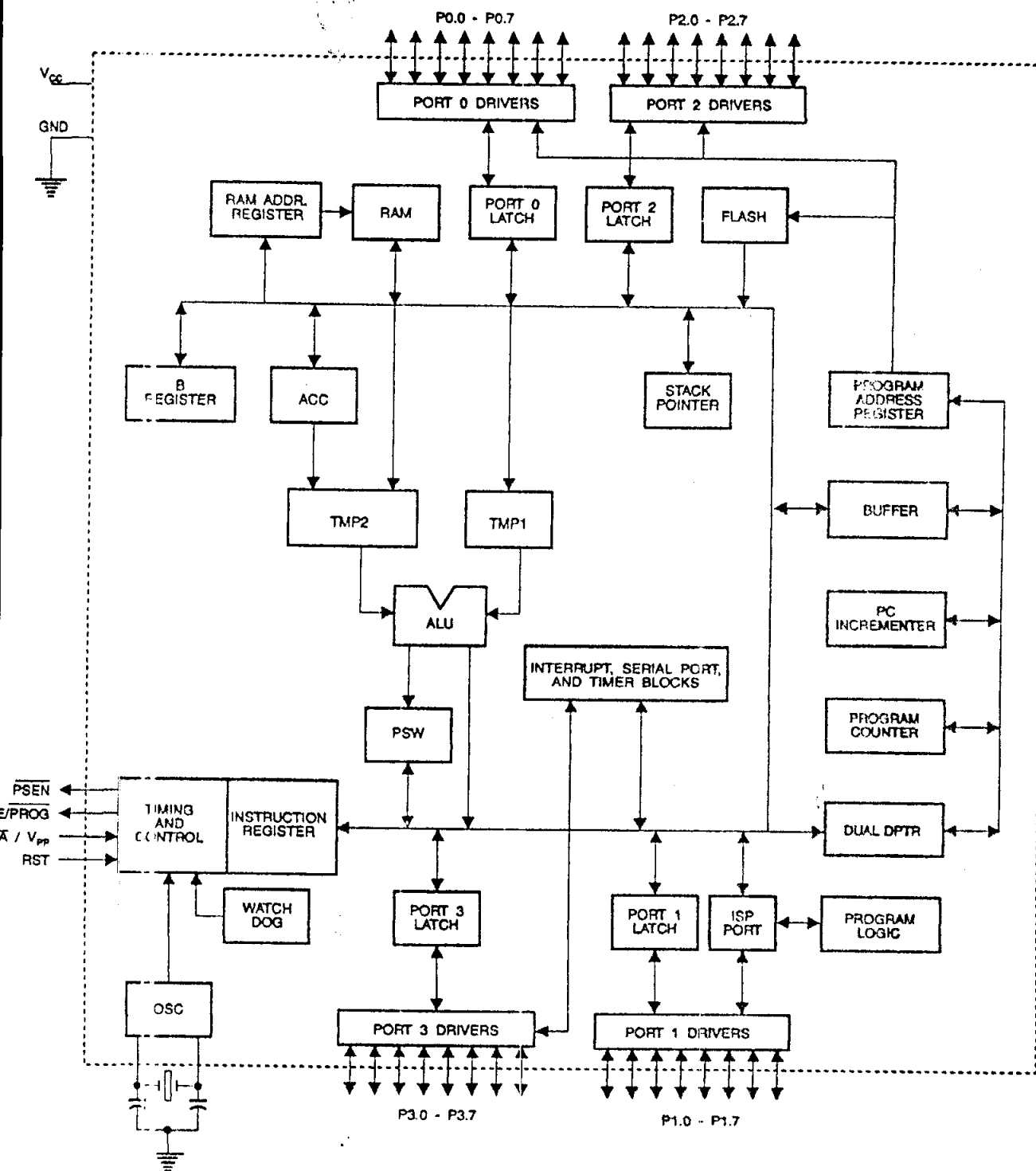
PLCC



TQFP



Block Diagram





Port Description

Port C

Supply voltage.

Port D

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable (PSEN) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

F8H								0FFH
F0H	B 00000000							0F7H
E8H								0EFH
E0H	ACC 00000000							0E7H
D8H								0DFH
D0H	PSW 00000000							0D7H
C8H								0CFH
C0H								0C7H
B8H	IP XX000000							0BFH
B0H	P3 11111111							0B7H
A8H	IE 0X000000							0AFH
A0H	P2 11111111		AUXR1 XXXXXXXX0			WDRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111							97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR

Address = 8EH

Reset Value = XXX00XX0B

Not Bit
Addressable

	—	—	—	WDIDLE	DISRTO	—	—	DISALE
Bit	7	6	5	4	3	2	1	0

—

Reserved for future expansion

DISALE

Disable/Enable ALE

 DISALE
 Operating Mode

0

ALE is emitted at a constant rate of 1/6 the oscillator frequency

1

ALE is active only during a MOVX or MOVC instruction

DISRTO

Disable/Enable Reset out

 DISRTO

0

Reset pin is driven High after WDT times out

1

Reset pin is input only

WDIDLE

Disable/Enable WDT in IDLE mode

WDIDLE

0

WDT continues to count in IDLE mode

1

WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.



Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1							
Address = A2H							
Reset Value = XXXXXXX0B							
Not Bit Addressable							
	-	-	-	-	-	-	DPS
Bit	7	6	5	4	3	2	1
-	Reserved for future expansion						
DPS	Data Pointer Register Select						
	DPS						
0	Selects DPTR Registers DP0L, DP0H						
1	Selects DPTR Registers DP1L, DP1H						

Memory Organization

Program Memory

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

If the \overline{EA} pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if \overline{EA} is connected to V_{CC} , program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (WDT) (Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

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The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register

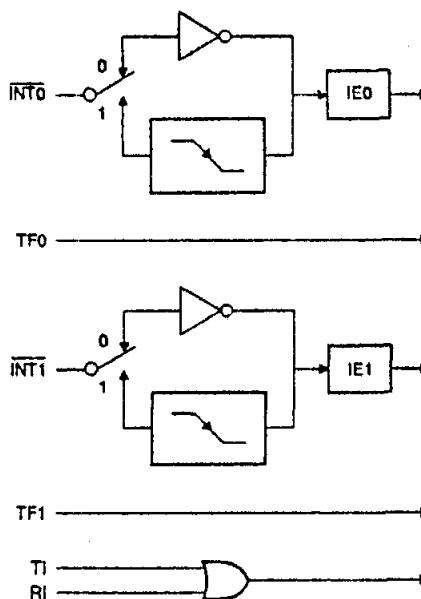
(MSB)				(LSB)			
EA	-	-	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved
-	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

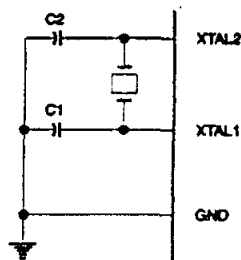
Figure 1. Interrupt Sources



Oscillator Characteristics

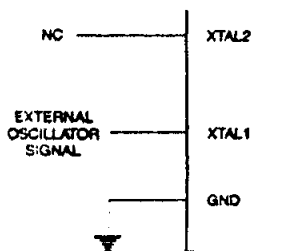
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF \pm 10 pF for Crystals = 40 pF \pm 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into INT0 or INT1. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.



Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVX instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/V_{PP} to 12V.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μ s. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S51 features Data Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel

(100H) = 51H indicates 89S51

(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
 Apply power between VCC and GND pins.
 Set RST pin to "H".
 If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.



Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set






The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Mode	V _{CC}	RST	PSEN	ALE/ PROG	EA/ V _{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
Write Code Data	5V	H	L		12V	L	H	H	H	H	D _{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D _{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L		12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L		12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L		12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L		12V	H	L	H	L	L	X	X	X
Read Atnel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

- Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
 2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
 3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
 4. RDY/BSY signal is output on P3.0 during programming.
 5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

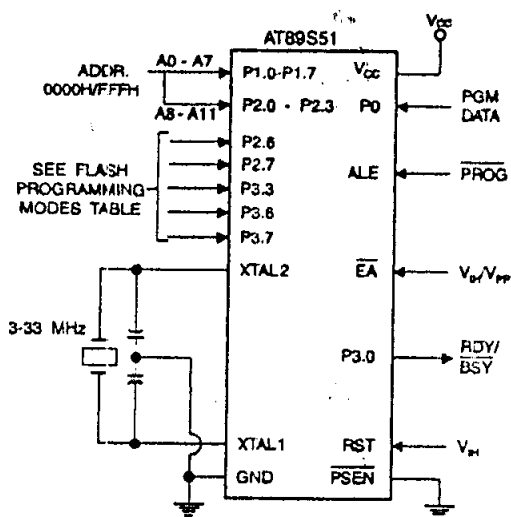
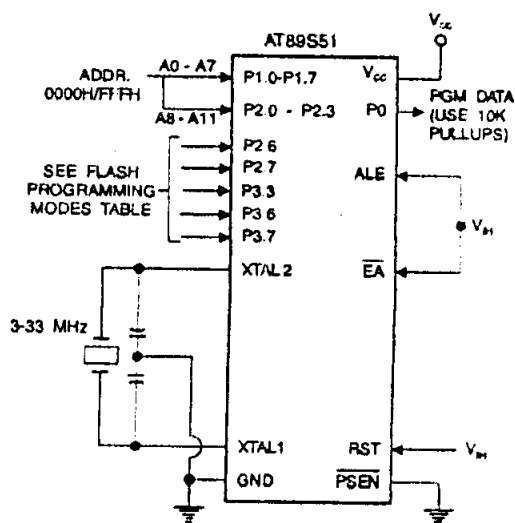


Figure 5. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

$T_A = 20^\circ\text{C}$ to 30°C , $V_{CC} = 4.5$ to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to \overline{PROG} Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After \overline{PROG}	$48t_{CLCL}$		
t_{DVGL}	Data Setup to \overline{PROG} Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After \overline{PROG}	$48t_{CLCL}$		
t_{ENSH}	P2.7 (\overline{ENABLE}) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to \overline{PROG} Low	10		μs
t_{GHSL}	V_{PP} Hold After \overline{PROG}	10		μs
t_{GLGH}	\overline{PROG} Width	0.2	1	μs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	\overline{ENABLE} Low to Data Valid		$48t_{CLCL}$	
t_{EHOZ}	Data Float After \overline{ENABLE}	0	$48t_{CLCL}$	
t_{GHBL}	\overline{PROG} High to \overline{BUSY} Low		1.0	μs
t_{WC}	Byte Write Cycle Time		50	μs

Figure 6. Flash Programming and Verification Waveforms – Parallel Mode

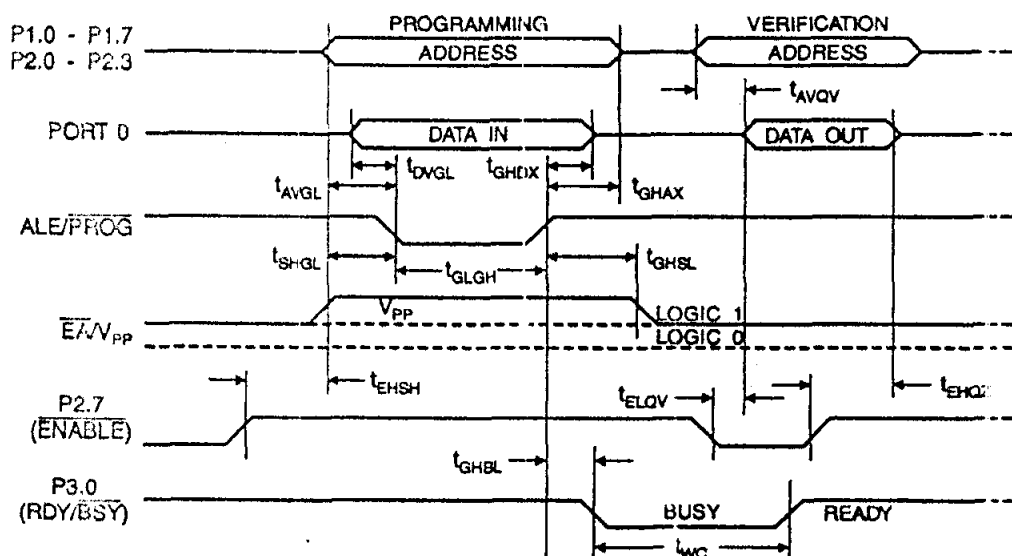
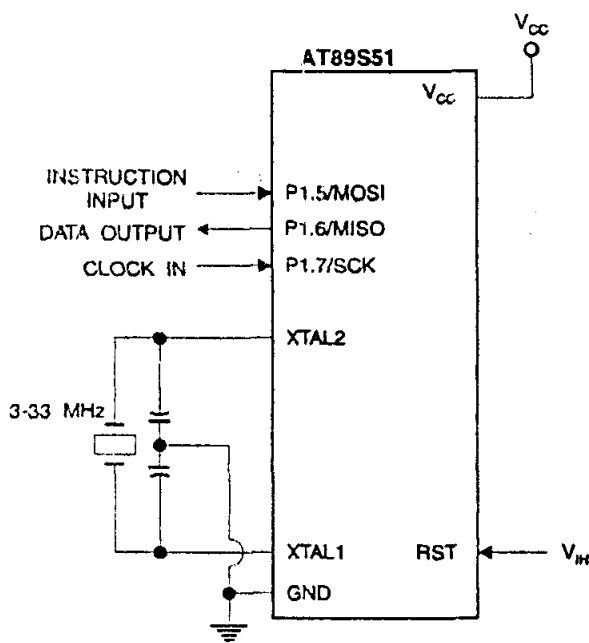


Figure 7. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 8. Serial Programming Waveforms

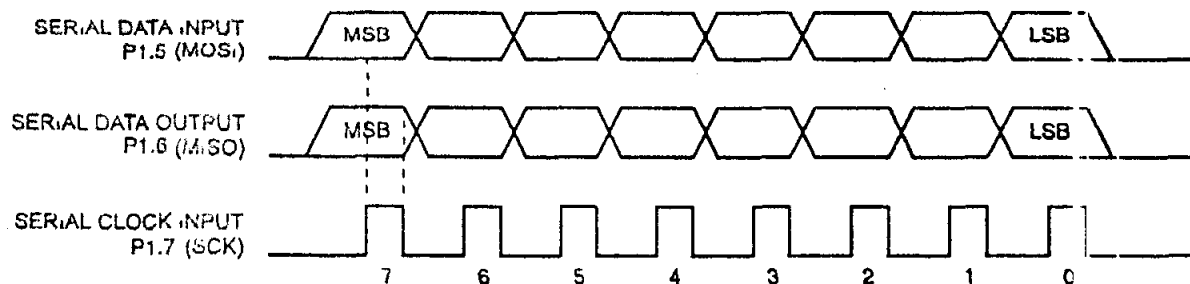


Table 8. Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	Write data to Program memory in the byte mode
Write Lock Bits ⁽²⁾	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx B3 B2 B1 B0 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes ⁽¹⁾	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 1 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
 B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
 B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
 B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

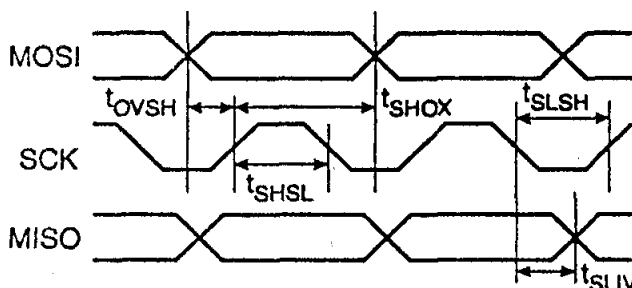
Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

Table 9. Serial Programming Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 4.0$ to 5.5V (unless otherwise noted))

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	$8 t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$8 t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2 t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			$64 t_{CLCL} + 400$	μs

Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.6V
DC Output Current.....	15.0 mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 4.0\text{V}$ to 5.5V , unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except EA)	-0.5	$0.2 V_{CC} - 0.1$	V
V_{IL1}	Input Low Voltage (EA)		-0.5	$0.2 V_{CC} - 0.3$	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} - 0.5$	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} - 0.5$	V
V_{OL}	Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
V_{OL1}	Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -800 \mu\text{A}, V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}, V_{CC} = 5\text{V} \pm 10\%$		-650	μA
I_{LI}	Input Leakage Current (Port 0, EA)	$0.45 < V_{IN} < V_{CC}$		± 10	μA
RRST	Reset Pulldown Resistor		50	300	$\text{K}\Omega$
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽²⁾	$V_{CC} = 5.5\text{V}$		50	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port:

Port 0: 26 mA Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.

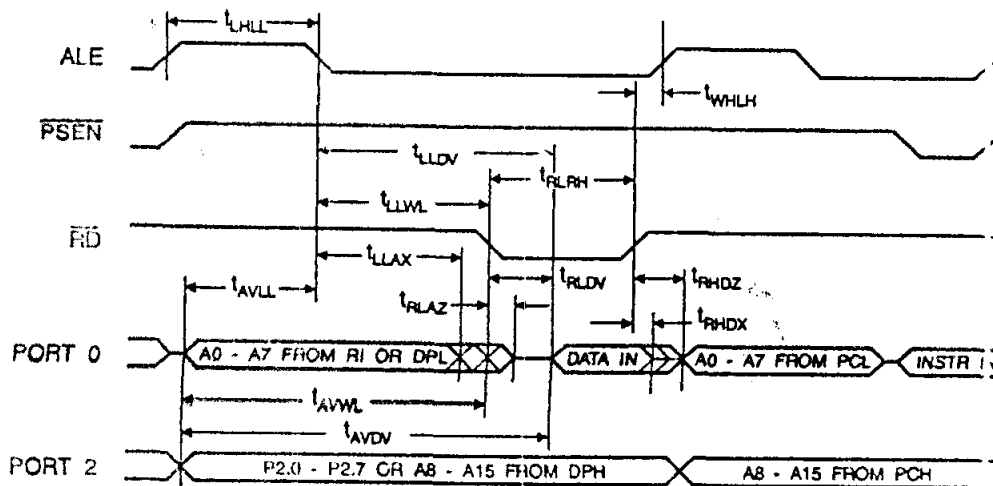
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other outputs = 80 pF.

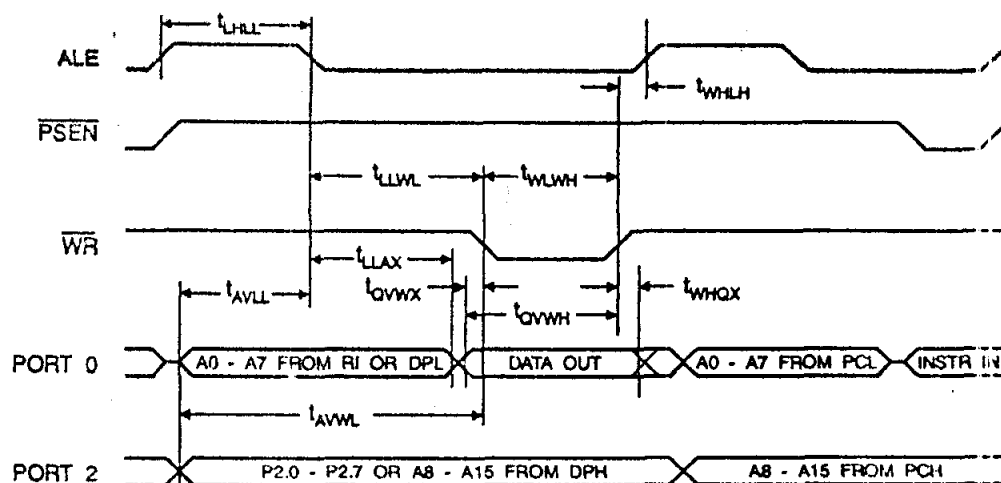
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/ t_{CLCL}	Oscillator Frequency			0	33	MHz
t_{HLH}	ALE Pulse Width	127		$2t_{CLCL}-40$		ns
t_{AVLL}	Address Valid to ALE Low	43		$t_{CLCL}-25$		ns
t_{LAX}	Address Hold After ALE Low	48		$t_{CLCL}-25$		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}-65$	ns
t_{LLPL}	ALE Low to PSEN Low	43		$t_{CLCL}-25$		ns
t_{PLPH}	PSEN Pulse Width	205		$3t_{CLCL}-45$		ns
t_{PLIV}	PSEN Low to Valid Instruction In		145		$3t_{CLCL}-60$	ns
t_{PXIX}	Input Instruction Hold After PSEN	0		0		ns
t_{PXIZ}	Input Instruction Float After PSEN		59		$t_{CLCL}-25$	ns
t_{PXAV}	PSEN to Address Valid	75		$t_{CLCL}-8$		ns
t_{AVIV}	Address to Valid Instruction In		312		$6t_{CLCL}-80$	ns
t_{PLAZ}	PSEN Low to Address Float		10		()	ns
t_{RLMH}	RD Pulse Width	400		$6t_{CLCL}-100$		ns
t_{WLWH}	WR Pulse Width	400		$6t_{CLCL}-100$		ns
t_{RLDV}	RD Low to Valid Data In		252		$5t_{CLCL}-90$	ns
t_{RHDX}	Data Hold After RD	0		0		ns
t_{RHDZ}	Data Float After RD		97		$2t_{CLCL}-23$	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}-150$	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}-165$	ns
t_{LLWL}	ALE Low to RD or WR Low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to RD or WR Low	203		$4t_{CLCL}-75$		ns
t_{QVWX}	Data Valid to WR Transition	23		$t_{CLCL}-30$		ns
t_{QVWH}	Data Valid to WR High	433		$7t_{CLCL}-130$		ns
t_{WHDX}	Data Hold After WR	33		$t_{CLCL}-25$		ns
t_{RLAZ}	RD Low to Address Float		0		()	ns
t_{WHLH}	RD or WR High to ALE High	43	123	$t_{CLCL}-25$	$t_{CLCL}+25$	ns

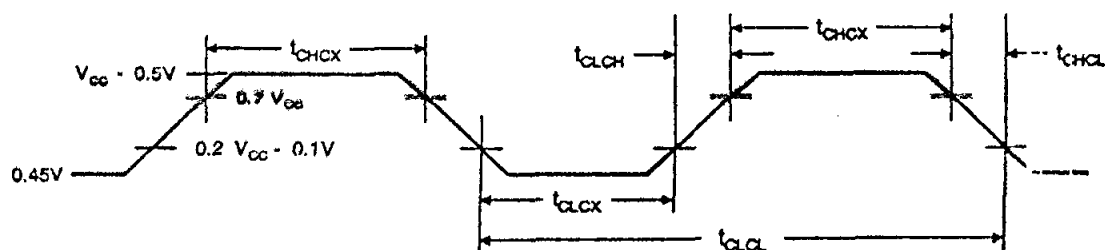
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms

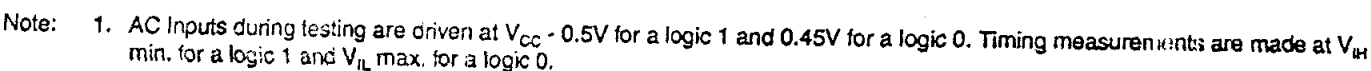


External Clock Drive

Symbol	Parameter	Min	Max	Units
1/f _{CLCL}	Oscillator Frequency	0	33	MHz
t _{CLCL}	Clock Period	30		ns
t _{CHCX}	High Time	12		ns
t _{CLCX}	Low Time	12		ns
t _{CLCH}	Rise Time		5	ns
t _{CHCL}	Fall Time		5	ns

The values in this table are valid for $V_{CC} = 4.0V$ to $5.5V$ and Load Capacitance = 80 pF.


Shift Register Mode Timing Waveforms



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

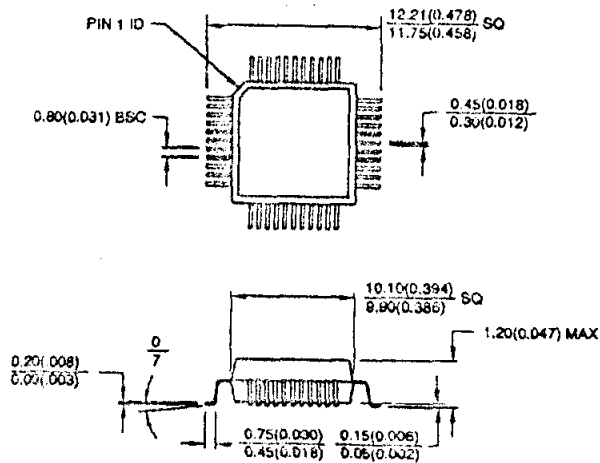
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC	44A	Commercial (0°C to 70°C)
		AT89S51-24JC	44J	
		AT89S51-24PC	40P6	
		AT89S51-24AI	44A	Industrial (-40°C to 85°C)
		AT89S51-24JI	44J	
		AT89S51-24PI	40P6	
33	4.5V to 5.5V	AT89S51-33AC	44A	Commercial (0°C to 70°C)
		AT89S51-33JC	44J	
		AT89S51-33PC	40P6	

 = Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

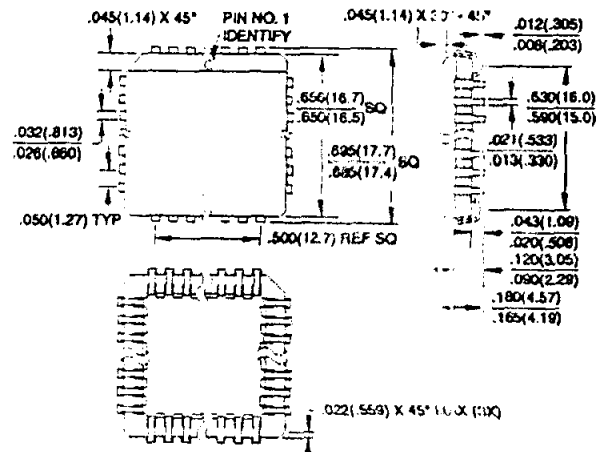
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
 Dimensions in Millimeters and (Inches)*

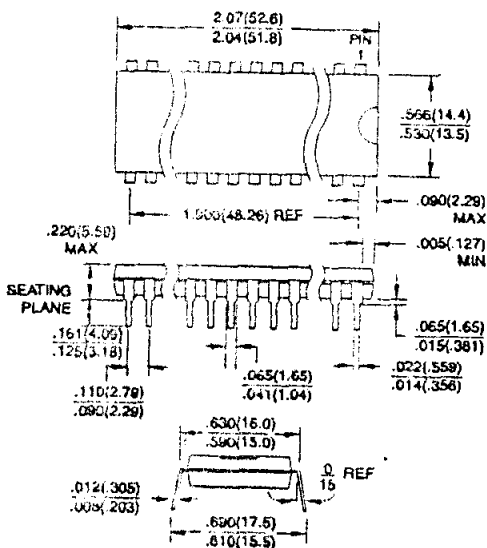


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-011 AC





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2487A-10/01/xm

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively



TO-126
1. Emitter 2. Collector 3. Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CB0}	Collector-Base Voltage : BD135	45	V
	: BD137	60	V
	: BD139	80	V
V_{CEO}	Collector-Emitter Voltage : BD135	45	V
	: BD137	60	V
	: BD139	80	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	1.5	A
I_{CP}	Collector Current (Pulse)	3.0	A
I_B	Base Current	0.5	A
P_C	Collector Dissipation ($T_C=25^\circ\text{C}$)	12.5	W
P_C	Collector Dissipation ($T_J=25^\circ\text{C}$)	1.25	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 ~ 150	$^\circ\text{C}$

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units	
$V_{CE(sat)}$	Collector-Emitter Saturated Voltage						
	: BD135	$I_C = 30\text{mA}, I_B = 0$	45			V	
	: BD137		60			V	
	: BD139		80			V	
I_{CBO}	Collector Cut-off Current	$V_{CB} = 30\text{V}, I_E = 0$			0.1	μA	
I_{EBO}	Emitter Cut-off Current	$V_{EB} = 5\text{V}, I_C = 0$			10	μA	
h_{FE1}	DC Current Gain : ALL DEVICE	$V_{CE} = 2\text{V}, I_C = 5\text{mA}$	25				
h_{FE2}		: ALL DEVICE	$V_{CE} = 2\text{V}, I_C = 0.5\text{A}$	25			
h_{FE3}		: BD135	$V_{CE} = 2\text{V}, I_C = 150\text{mA}$	40		25	
		: BD137, BD139		40		16	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 500\text{mA}, I_B = 50\text{mA}$			0.1	V	
$V_{BE(on)}$	Base-Emitter ON Voltage	$V_{CE} = 2\text{V}, I_C = 0.5\text{A}$			1	V	

h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

Typical Characteristics

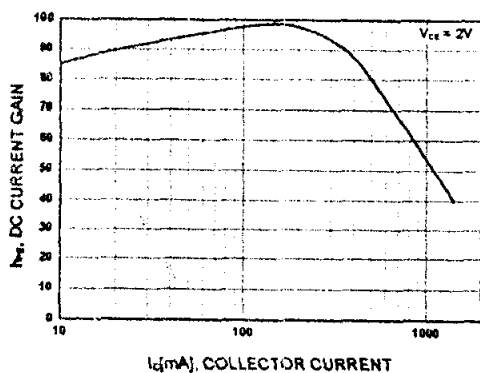


Figure 1. DC current Gain

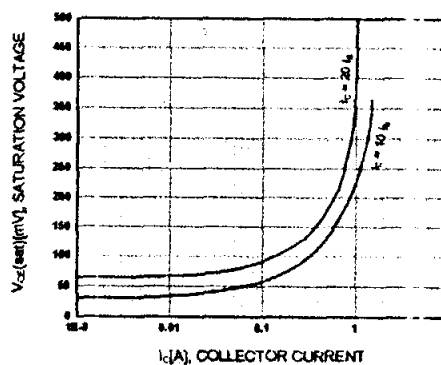
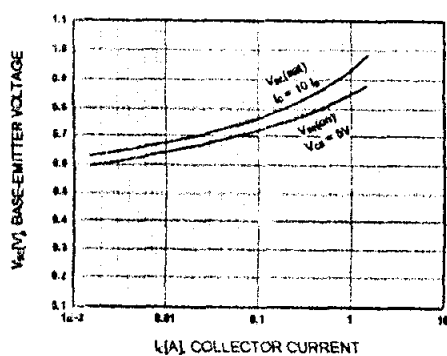
Figure 2. Collector-Emitter Saturation $V_{CE(sat)}$ 

Figure 3. Base-Emitter Voltage

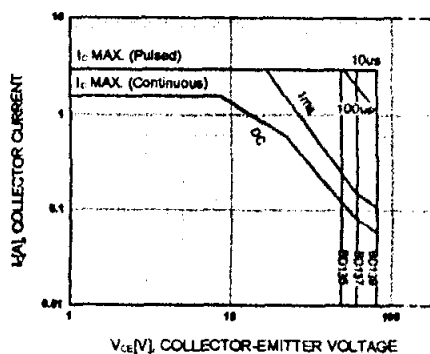


Figure 4. Safe Operating Area

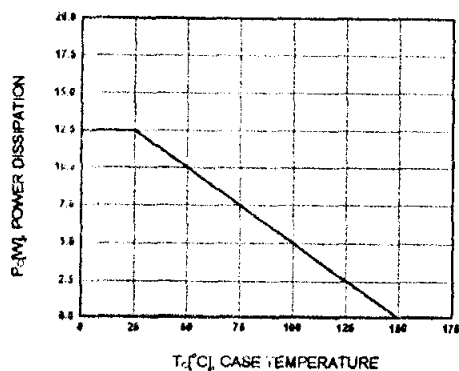
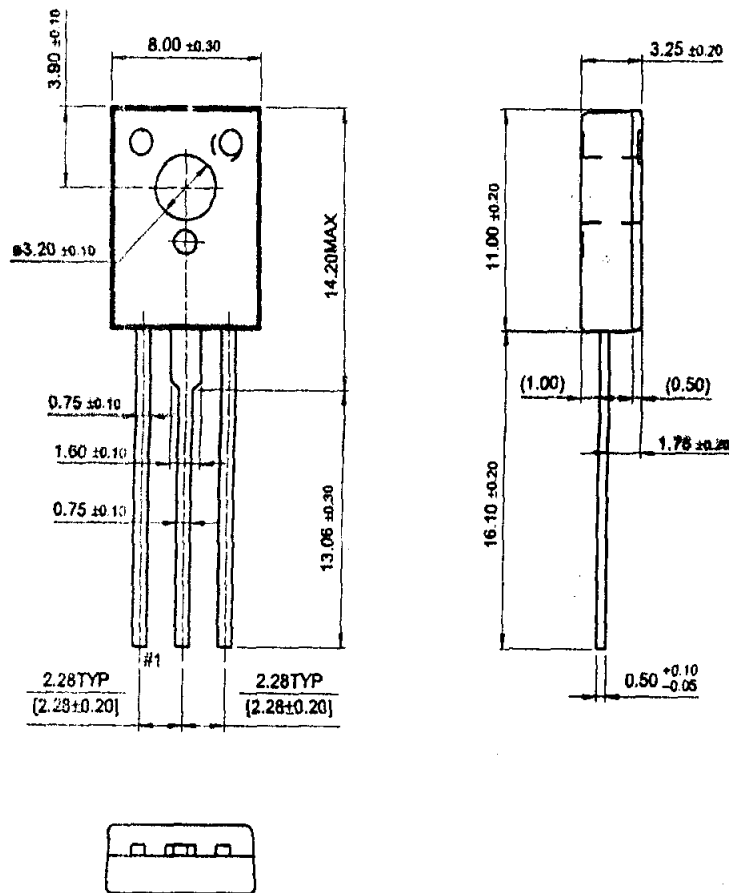


Figure 5. Power Derating

Package Dimensions

TO-126

BD135/137/139



Dimensions in millimeters

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Bottomless™	ISOPLANAR™	SyncFET™
CoolFET™	MICROWIRE™	TinyLogic™
CROSSVOLT™	POP™	UHC™
E ² CMOS™	PowerTrench®	VCX™
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

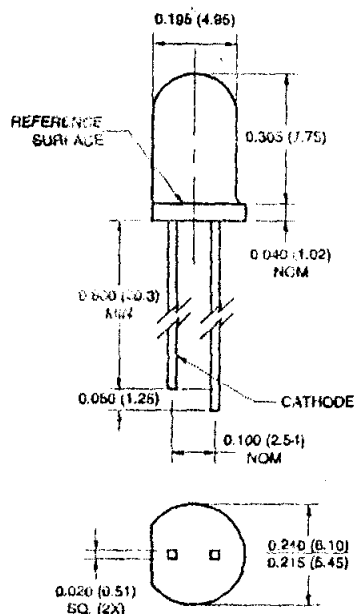
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

QED121/122/123

PLASTIC INFRARED LIGHT EMITTING DIODE

PACKAGE DIMENSIONS



NOTES:

1. Dimensions for all drawings are in inches (mm).
2. Tolerance of $\pm .010$ (.25) on all non-nominal dimensions unless otherwise specified.

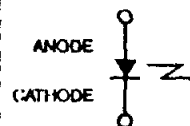
FEATURES

- $\lambda = 880$ nm
- Chip material = AlGaAs
- Package type: T-1 3/4 (5mm lens diameter)
- Matched Photosensor: QSD122/123/124
- Narrow Emission Angle, 18°
- High Output Power
- Package material and color: Clear, peach tinted, plastic



1. Derate power dissipation linearly 2.67 mW/°C above 25°C.
2. RMA flux is recommended.
3. Methanol or isopropyl alcohols are recommended as cleaning agents.
4. Soldering iron 1/16" (1.6mm) minimum from housing.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Operating Temperature	T_{OPR}	-40 to +100	$^\circ\text{C}$
Storage Temperature	T_{STG}	-40 to +100	$^\circ\text{C}$
Soldering Temperature (Iron)(2,3,4)	T_{SOL-I}	240 for 5 sec	$^\circ\text{C}$
Soldering Temperature (Flow)(2,3)	T_{SOL-F}	260 for 10 sec	$^\circ\text{C}$
Continuous Forward Current	I_F	100	mA
Reverse Voltage	V_R	5	V
Power Dissipation(1)	P_D	200	mW

ELECTRICAL / OPTICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Peak Emission Wavelength	$I_F = 20$ mA	λ_{PE}	—	880	—	nm
Emission Angle	$I_F = 100$ mA	θ	—	± 9	—	Deg.
Forward Voltage	$I_F = 100$ mA, $t_p = 20$ ms	V_F	—	—	1.7	V
Reverse Current	$V_R = 5$ V	I_R	—	—	10	μA
Radiant Intensity QED121	$I_F = 100$ mA, $t_p = 20$ ms	I_E	16	—	40	mW/sr
Radiant Intensity QED122	$I_F = 100$ mA, $t_p = 20$ ms	I_E	32	—	100	mW/sr
Radiant Intensity QED123	$I_F = 100$ mA, $t_p = 20$ ms	I_E	50	—	—	mW/sr
Rise Time	$I_F = 100$ mA	t_r	—	800	—	ns
Fall Time	$I_F = 100$ mA	t_f	—	800	—	ns

TYPICAL PERFORMANCE CURVES

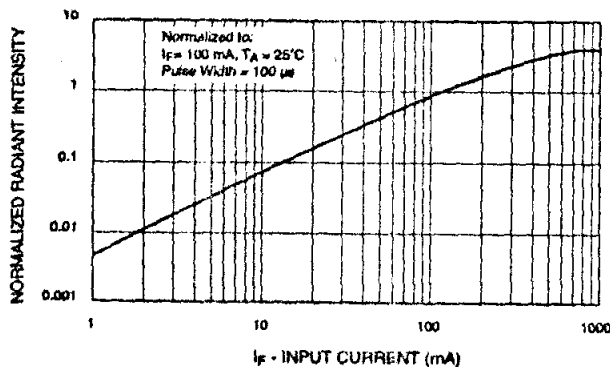


Fig. 1 Normalized Radiant Intensity vs. Input Current

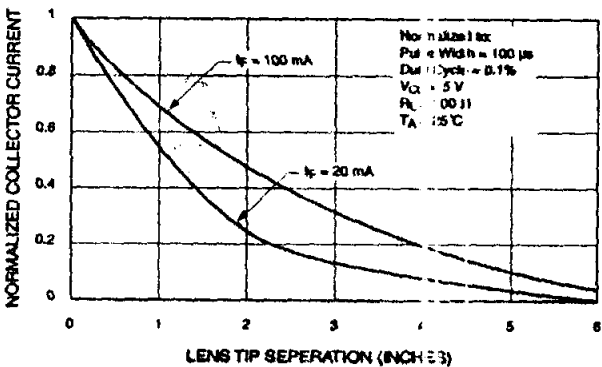


Fig. 2 Coupling Characteristics of QED121 and QSD12X

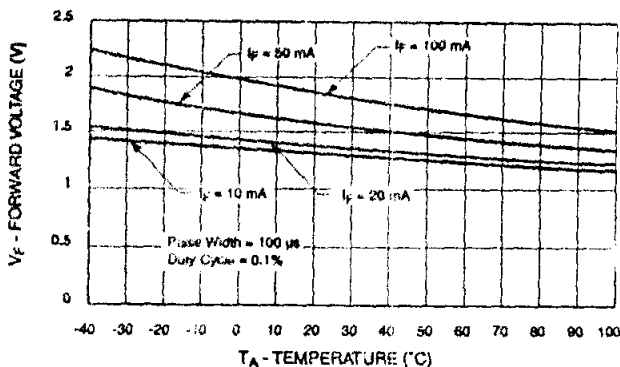


Fig. 3 Forward Voltage vs. Temperature

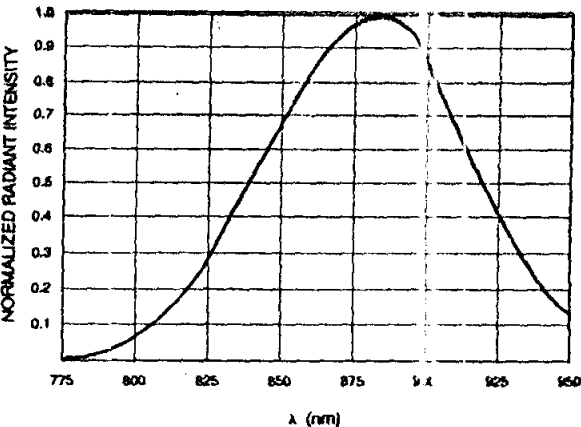


Fig. 4 Normalized Radiant Intensity vs. Wavelength

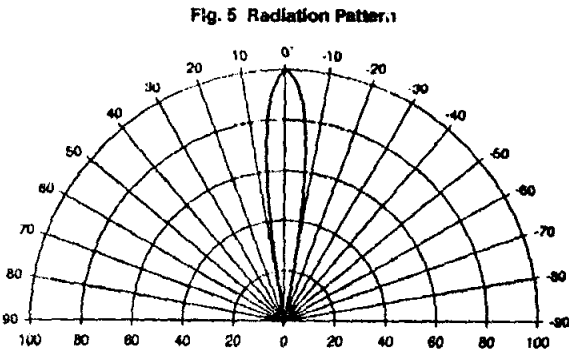


Fig. 5 Radiation Pattern

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

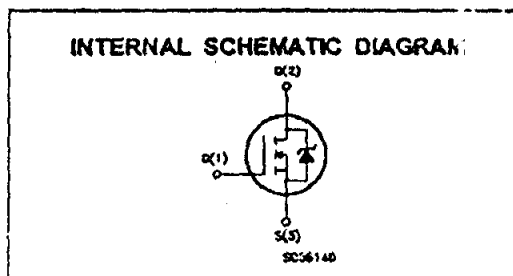
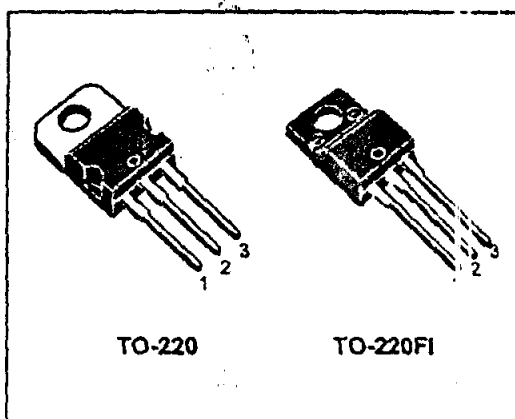
N - CHANNEL 100V - 0.050Ω - 30A - TO-220/TO-220FI POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
IRF540	100 V	< 0.077 Ω	30 A
IRF540FI	100 V	< 0.077 Ω	16 A

- TYPICAL R_{DS(on)} = 0.050 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- DC-DC & DC-AC CONVERTER
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMP DRIVERS Etc.)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		IRF530	IRF530FI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100		V
V _{GS}	Gate-source Voltage	± 20		V
I _D	Drain Current (continuous) at T _c = 25 °C	30	17	A
I _D	Drain Current (continuous) at T _c = 100 °C	21	12	A
I _{DM} (*)	Drain Current (pulsed)	120	120	A
P _{tot}	Total Dissipation at T _c = 25 °C	150	45	W
	Derating Factor	1	0.3	W/°C
V _{iso}	Insulation Withstand Voltage (DC)	-	2000	V
T _{stg}	Storage Temperature	-65 to 175		°C
T _j	Max. Operating Junction Temperature	175		°C

(*) Pulse width limited by safe operating area

(1) I_{SD} ≤ 30 A, di/dt ≤ 200 A/μs, V_{DS} ≤ V_{DSS}, T_J ≤ T_{MAX}

THERMAL DATA

			TO-220	TO220-FI	
$R_{thj-case}$	Thermal Resistance Junction-case	Max	1	3.33	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5		$^{\circ}\text{C/W}$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.5		$^{\circ}\text{C/W}$
T_l	Maximum Lead Temperature For Soldering Purpose		300		$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_J max)	30	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_J = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	200	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}$		0.05	0.077	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	30			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 15\text{ A}$	10	20		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		2600	3600	pF
C_{oss}	Output Capacitance			350	500	pF
C_{riss}	Reverse Transfer Capacitance			85	120	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 50\text{ V}$ $I_D = 15\text{ A}$		20	28	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		60	85	ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}$		80	110	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			28		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(voff)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 30\text{ A}$		22	30	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		25	35	ns
t_c	Cross-over Time			55	75	ns

SOURCE DRAIN DIODE

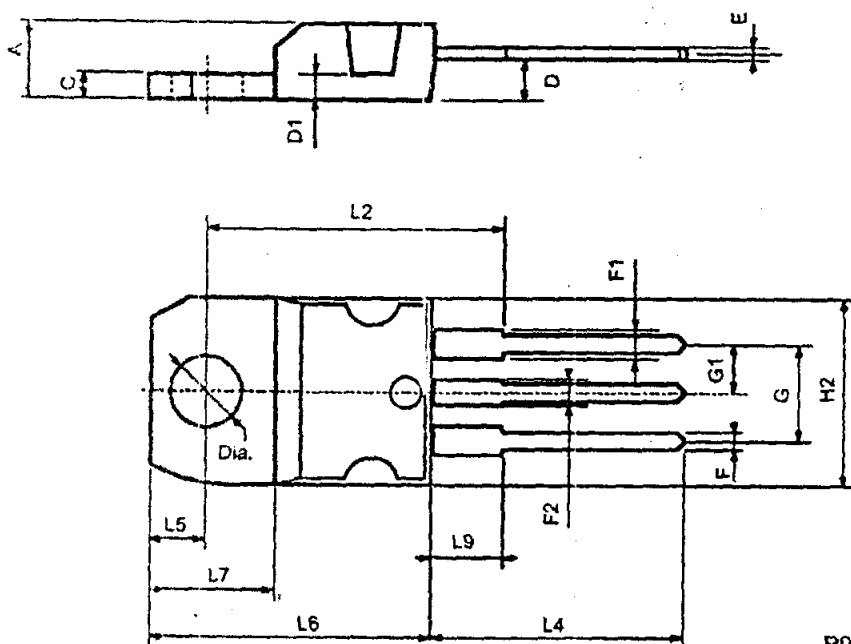
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				30	A
$I_{SDM}(*)$	Source-drain Current (pulsed)				120	A
$V_{SD}(*)$	Forward On Voltage	$I_{SD} = 50\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 30\text{ A}$ $dI/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150^\circ\text{C}$		175		ns
Q_{rr}	Reverse Recovery Charge			1.1		μC
I_{RRM}	Reverse Recovery Current			12.5		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(*) Pulse width limited by safe operating area

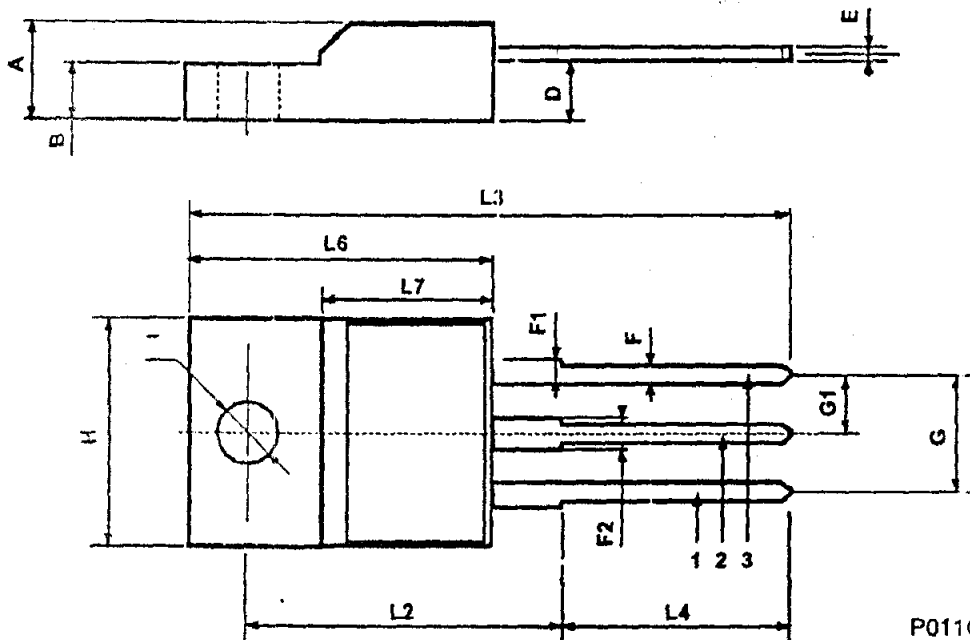
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.621
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.155
DIA.	3.75		3.85	0.147		0.151



ISOWATT220 MECHANICAL DATA

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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KA78XX/KA78XXA

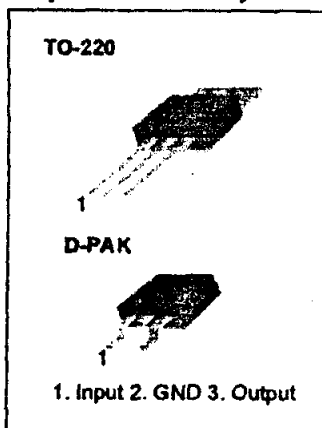
3-Terminal 1A Positive Voltage Regulator

Features

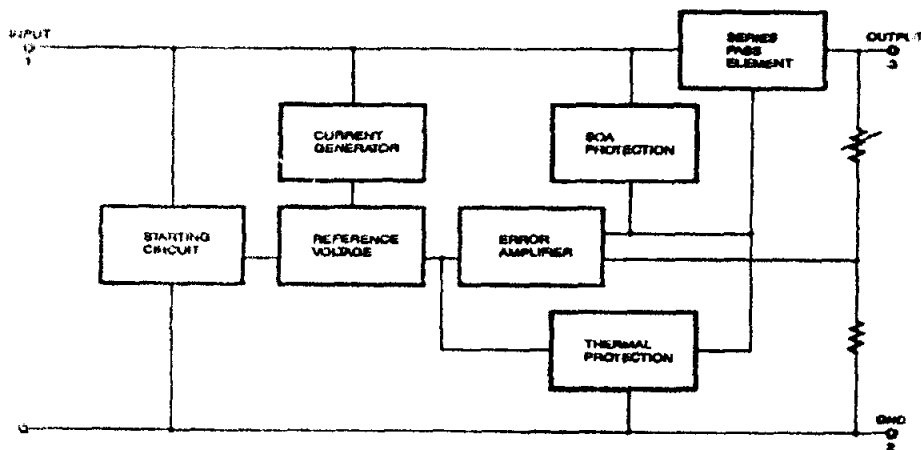
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The KA78XX/KA78XXA series of three-terminal positive regulator are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for $V_O = 5V$ to $18V$) (for $V_O = 24V$)	V_I	35	V
	V_I	40	V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	$^{\circ}C/W$
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	$^{\circ}C/W$
Operating Temperature Range (KA78XX/A/R)	T_{OPR}	$0 \sim +125$	$^{\circ}C$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^{\circ}C$

Electrical Characteristics (KA7805/KA7805R)

(Refer to test circuit, $0^{\circ}C < T_J < 125^{\circ}C$, $I_O = 500mA$, $V_I = 10V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7805			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}C$	4.8	5.0	5.2	V
		$5.0mA \leq I_O \leq 1.0A$, $P_O \leq 15W$ $V_I = 7V$ to $20V$	4.75	5.0	5.25	
Line Regulation (Note1)	Reg_{line}	$T_J = +25^{\circ}C$	$V_O = 7V$ to $25V$		100	mV
			$V_I = 8V$ to $12V$		50	
Load Regulation (Note1)	Reg_{load}	$T_J = +25^{\circ}C$	$I_O = 5.0mA$ to $1.5A$		100	mV
			$I_O = 250mA$ to $750mA$		50	
Quiescent Current	I_Q	$T_J = +25^{\circ}C$	-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	$I_Q = 5mA$ to $1.0A$	-	0.03	0.5	mA
		$V_I = 7V$ to $25V$	-	0.3	1.3	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5mA$	-	-0.8	-	mV/ $^{\circ}C$
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $T_A = +25^{\circ}C$	-	42	-	$\mu V/V_O$
Ripple Rejection	RR	$f = 120Hz$ $V_O = 8V$ to $18V$	62	73	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1A$, $T_J = +25^{\circ}C$	-	2	-	V
Output Resistance	r_O	$f = 1KHz$	-	15	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35V$, $T_A = +25^{\circ}C$	-	230	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}C$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7806/KA7806R)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 11\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7803			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	5.75	6.0	6.25	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 8.0\text{V to } 21\text{V}$	5.7	6.0	6.3	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$	$V_I = 8\text{V to } 25\text{V}$		120	mV
			$V_I = 9\text{V to } 13\text{V}$		60	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$	$I_O = 5\text{mA to } 1.5\text{A}$		120	mV
			$I_O = 250\text{mA to } 750\text{mA}$		60	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1\text{A}$	-	-	0.5	mA
		$V_I = 8\text{V to } 25\text{V}$	-	-	1.3	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-0.8	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$, $T_A = +25^{\circ}\text{C}$	-	45	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 9\text{V to } 19\text{V}$	59	75	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	19	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7808/KA7808R)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 14\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions		KA7808			Unit
				Min.	Typ.	Max.	
Output Voltage	Vo	TJ =+25 °C		7.7	8.0	8.3	V
		5.0mA ≤ IO ≤ 1.0A, PO ≤ 15W VI = 10.5V to 23V		7.6	8.0	8.4	
Line Regulation (Note1)	Regline	TJ =+25 °C	VI = 10.5V to 25V	-	5.0	160	mV
			VI = 11.5V to 17V	-	2.0	80	
Load Regulation (Note1)	Regload	TJ =+25 °C	IO = 5.0mA to 1.5A	-	10	160	mV
			IO= 250mA to 750mA	-	5.0	80	
Quiescent Current	IQ	TJ =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔIQ	IO = 5mA to 1.0A		-	0.05	0.5	mA
		VI = 10.5A to 25V		-	0.5	1.0	
Output Voltage Drift	ΔVO/ΔT	IO = 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 100KHz, TA =+25 °C		-	52	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, VI= 11.5V to 21.5V		56	73	-	dB
Dropout Voltage	VDrop	IO = 1A, TJ=+25 °C		-	2	-	V
Output Resistance	ro	f = 1KHz		-	17	-	mΩ
Short Circuit Current	ISC	VI= 35V, TA =+25 °C		-	230	-	mA
Peak Current	IPK	TJ =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7809/KA7809R)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 15\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions		KA78XX			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$		8.65	9	9.35	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 11.5\text{V to } 24\text{V}$		8.6	9	9.4	
Line Regulation (Note1)	R_{glne}	$T_J = +25^{\circ}\text{C}$	$V_I = 11.5\text{V to } 25\text{V}$	-	6	180	mV
			$V_I = 12\text{V to } 17\text{V}$	-	2	90	
Load Regulation (Note1)	R_{ugload}	$T_J = +25^{\circ}\text{C}$	$I_O = 5\text{mA to } 1.5\text{A}$	-	12	180	mV
			$I_O = 250\text{mA to } 750\text{mA}$	-	4	90	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$		-	-	0.5	mA
		$V_I = 11.5\text{V to } 26\text{V}$		-	-	1.3	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$		-	-1	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = +25^{\circ}\text{C}$		-	58	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 13\text{V to } 23\text{V}$		56	71	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$		-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$		-	17	-	m Ω
Short Circuit Current	ISC	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$		-	250	-	mA
Peak Current	IPK	$T_J = +25^{\circ}\text{C}$		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7810)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 16\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7810			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	9.6	10	10.4	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 12.5\text{V to } 25\text{V}$	9.5	10	10.5	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$				mV
		$V_I = 12.5\text{V to } 25\text{V}$	-	10	20	
		$V_I = 13\text{V to } 25\text{V}$	-	3	10	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$				mV
		$I_O = 5\text{mA to } 1.5\text{A}$	-	12	20	
		$I_O = 250\text{mA to } 750\text{mA}$	-	4	40	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	mA
		$V_I = 12.5\text{V to } 29\text{V}$	-	-	1.0	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-1	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = +25^{\circ}\text{C}$	-	58	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 13\text{V to } 23\text{V}$	56	71	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	17	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7812/KA7812R)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 19\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7812/KA7812R			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	11.5	12	12.5	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 14.5\text{V to } 27\text{V}$	11.4	12	12.6	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$	$V_I = 14.5\text{V to } 30\text{V}$		240	mV
			$V_I = 16\text{V to } 22\text{V}$		120	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$	$I_O = 5\text{mA to } 1.5\text{A}$		240	mV
			$I_O = 250\text{mA to } 750\text{mA}$		120	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$	-	0.1	0.5	mA
		$V_I = 14.5\text{V to } 30\text{V}$	-	0.5	1.0	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-1	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = +25^{\circ}\text{C}$	-	78	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 15\text{V to } 25\text{V}$	55	71	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	18	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	230	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7815)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 23\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7815			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	14.4	15	15.6	V
		$5.0\text{mA} \leq I_{OS} \leq 1.0\text{A}$, $P_{OS} \leq 15\text{W}$ $V_I = 17.5\text{V to } 30\text{V}$	14.25	15	15.75	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$	-	11	300	mV
		$V_I = 17.5\text{V to } 30\text{V}$ $V_I = 20\text{V to } 28\text{V}$			150	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$	-	12	300	mV
		$I_O = 5\text{mA to } 1.5\text{A}$ $I_O = 250\text{mA to } 750\text{mA}$			150	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	mA
		$V_I = 17.5\text{V to } 30\text{V}$	-	-	1.0	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-1	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = +25^{\circ}\text{C}$	-	90	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 18.5\text{V to } 28.5\text{V}$	54	70	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	19	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7818)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 27\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7818			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	17.3	18	18.7	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 21\text{V to } 33\text{V}$	17.1	18	18.9	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$				mV
		$V_I = 21\text{V to } 33\text{V}$	-	15	360	
		$V_I = 24\text{V to } 30\text{V}$	-	5	180	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$				mV
		$I_O = 5\text{mA to } 1.5\text{A}$	-	15	360	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5.0	180	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	mA
		$V_I = 21\text{V to } 33\text{V}$	-	-	1	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-1	-	mV/°C
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$, $T_A = +25^{\circ}\text{C}$	-	110	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 22\text{V to } 32\text{V}$	53	69	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	22	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7824)

(Refer to test circuit, $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 500\text{mA}$, $V_I = 33\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	KA7824			Unit
			Min.	Typ.	Max.	
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	23	24	25	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$ $V_I = 27\text{V to } 38\text{V}$	22.8	24	25.25	
Line Regulation (Note1)	Regline	$T_J = +25^{\circ}\text{C}$	-	17	480	mV
		$V_I = 27\text{V to } 38\text{V}$ $V_I = 30\text{V to } 38\text{V}$			240	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$	-	15	480	mV
		$I_O = 5\text{mA to } 1.5\text{A}$ $I_O = 250\text{mA to } 750\text{mA}$			240	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$	-	0.1	0.5	mA
		$V_I = 27\text{V to } 38\text{V}$	-	0.5	1	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$	-	-1.5	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = +25^{\circ}\text{C}$	-	60	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 28\text{V to } 38\text{V}$	50	67	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	28	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	230	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7805A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 10\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	4.9	5	5.1	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 7.5\text{V to } 20\text{V}$	4.8	5	5.2	
Line Regulation (Note1)	Regline	$V_I = 7.5\text{V to } 25\text{V}$ $I_O = 500\text{mA}$	-	5	(5)	mV
		$V_I = 8\text{V to } 12\text{V}$	-	3	(5)	
		$T_J = +25^{\circ}\text{C}$	$V_I = 7.3\text{V to } 20\text{V}$	-	5	(5)
			$V_I = 8\text{V to } 12\text{V}$	-	1.5	(2.5)
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	9	100	mV
		$I_O = 5\text{mA to } 1\text{A}$	-	9	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	4	(5)	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	(5)	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1\text{A}$	-	-	(5)	mA
		$V_I = 8\text{V to } 25\text{V}$, $I_O = 500\text{mA}$	-	-	(3)	
		$V_I = 7.5\text{V to } 20\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	(3)	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-0.8	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 8\text{V to } 18\text{V}$	-	68	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	17	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7806A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 11\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	5.58	6	6.12	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 8.6\text{V to } 21\text{V}$	5.76	6	6.24	
Line Regulation (Note1)	Regline	$V_I = 8.6\text{V to } 25\text{V}$ $I_O = 500\text{mA}$	-	5	60	mV
		$V_I = 9\text{V to } 13\text{V}$	-	3	60	
		$T_J = +25^{\circ}\text{C}$	$V_I = 8.3\text{V to } 21\text{V}$	-	5	60
			$V_I = 9\text{V to } 13\text{V}$	-	1.5	60
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	9	100	mV
		$I_O = 5\text{mA to } 1\text{A}$	-	4	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5.0	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	4.3	6.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1\text{A}$	-	-	0.5	mA
		$V_I = 9\text{V to } 25\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$V_I = 8.5\text{V to } 21\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-0.8	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 9\text{V to } 19\text{V}$	-	65	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	17	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effect must be taken into account separately. Pulse testing with low duty is used

Electrical Characteristics (KA7808A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 14\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	7.84	8	8.16	V
		$I_O = 5\text{mA}$ to 1A , $P_O \leq 15\text{W}$ $V_I = 10.6\text{V}$ to 23V	7.7	8	8.3	
Line Regulation (Note1)	Regline	$V_I = 10.6\text{V}$ to 25V $I_O = 500\text{mA}$	-	6	80	mV
		$V_I = 11\text{V}$ to 17V	-	3	80	
		$T_J = +25^{\circ}\text{C}$	$V_I = 10.4\text{V}$ to 23V	-	8	80
			$V_I = 11\text{V}$ to 17V	-	2	40
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA}$ to 1.5A	-	12	100	mV
		$I_O = 5\text{mA}$ to 1A	-	12	100	
		$I_O = 250\text{mA}$ to 750mA	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A	-	-	0.5	mA
		$V_I = 11\text{V}$ to 25V , $I_O = 500\text{mA}$	-	-	0.8	
		$V_I = 10.6\text{V}$ to 23V , $T_J = +25^{\circ}\text{C}$	-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-0.8	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100kHz $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 11.5\text{V}$ to 21.5V	-	62	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	18	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7809A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 15\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	8.82	9.0	9.13	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 11.2\text{V to } 24\text{V}$	8.65	9.0	9.35	
Line Regulation (Note1)	Regline	$V_I = 11.7\text{V to } 25\text{V}$ $I_O = 500\text{mA}$	-	6	90	mV
		$V_I = 12.5\text{V to } 19\text{V}$	-	4	45	
		$T_J = +25^{\circ}\text{C}$	$V_I = 11.5\text{V to } 24\text{V}$	-	6	90
			$V_I = 12.5\text{V to } 19\text{V}$	-	2	45
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.0\text{A}$	-	12	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	12	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	3.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 11.7\text{V to } 25\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 12\text{V to } 25\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 12\text{V to } 22\text{V}$	-	62	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{kHz}$	-	17	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7810A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 16\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	9.8	10	10.2	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 12.8\text{V to } 25\text{V}$	9.6	10	10.4	
Line Regulation (Note1)	Regline	$V_I = 12.8\text{V to } 26\text{V}$ $I_O = 500\text{mA}$	-	8	100	mV
		$V_I = 13\text{V to } 20\text{V}$	-	4	50	
		$T_J = +25^{\circ}\text{C}$	$V_I = 12.5\text{V to } 25\text{V}$	-	8	100
			$V_I = 13\text{V to } 20\text{V}$	-	3	50
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	12	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	12	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 13\text{V to } 26\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.5	mA
		$V_I = 12.8\text{V to } 25\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 14\text{V to } 24\text{V}$	-	62	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	17	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effect must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7812A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 19\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	11.75	12	12.25	V
		$I_O = 5\text{mA}$ to 1A , $P_O \leq 15\text{W}$ $V_I = 14.8\text{V}$ to 27V	11.5	12	12.5	
Line Regulation (Note1)	Regline	$V_I = 14.8\text{V}$ to 30V $I_O = 500\text{mA}$	-	10	20	mV
		$V_I = 16\text{V}$ to 22V	-	4	20	
		$T_J = +25^{\circ}\text{C}$	$V_I = 14.5\text{V}$ to 27V	10	20	
			$V_I = 16\text{V}$ to 22V	3	30	
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA}$ to 1.5A	-	12	100	mV
		$I_O = 5\text{mA}$ to 1.0A	-	12	100	
		$I_O = 250\text{mA}$ to 750mA	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.1	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 15\text{V}$ to 30V , $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 14\text{V}$ to 27V , $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA}$ to 1.0A	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 14\text{V}$ to 24V	-	60	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	18	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7815A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 23\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	14.7	15	15.3	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 17.7\text{V to } 30\text{V}$	14.4	15	15.6	
Line Regulation (Note1)	Regline	$V_I = 17.9\text{V to } 30\text{V}$ $I_O = 500\text{mA}$	-	10	150	mV
		$V_I = 20\text{V to } 26\text{V}$	-	5	150	
		$T_J = +25^{\circ}\text{C}$	$V_I = 17.5\text{V to } 30\text{V}$	-	11	150
			$V_I = 20\text{V to } 26\text{V}$	-	3	75
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	12	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	12	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 17.5\text{V to } 30\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 17.5\text{V to } 30\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 18.5\text{V to } 28.5\text{V}$	-	58	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	19	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7818A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 27\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	17.64	18	18.36	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 21\text{V to } 33\text{V}$	17.3	18	18.7	
Line Regulation (Note1)	Regline	$V_I = 21\text{V to } 33\text{V}$ $I_O = 500\text{mA}$	-	15	180	mV
		$V_I = 21\text{V to } 33\text{V}$	-	5	180	
		$T_J = +25^{\circ}\text{C}$	$V_I = 20.6\text{V to } 33\text{V}$	-	15	180
			$V_I = 24\text{V to } 30\text{V}$	-	5	90
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	15	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	15	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	7	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 21\text{V to } 33\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 21\text{V to } 33\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 22\text{V to } 32\text{V}$	-	57	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	19	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (KA7824A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 33\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	23.5	24	24.5	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 27.3\text{V to } 38\text{V}$	23	24	25	
Line Regulation (Note1)	Regline	$V_I = 27\text{V to } 38\text{V}$ $I_O = 500\text{mA}$	-	18	240	mV
		$V_I = 21\text{V to } 33\text{V}$	-	6	240	
		$T_J = +25^{\circ}\text{C}$	$V_I = 26.7\text{V to } 38\text{V}$	-	18	240
			$V_I = 30\text{V to } 36\text{V}$	-	6	120
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	15	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	15	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	7	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 27.3\text{V to } 38\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 27.3\text{V to } 38\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.5	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = 25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 28\text{V to } 38\text{V}$	-	54	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	20	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effect must be taken into account separately. Pulse testing with low duty is used.

Typical Performance Characteristics

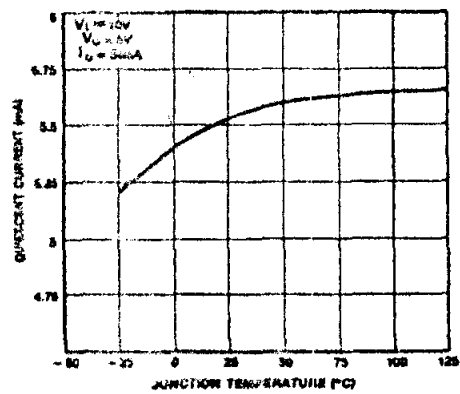


Figure 1. Quiescent Current

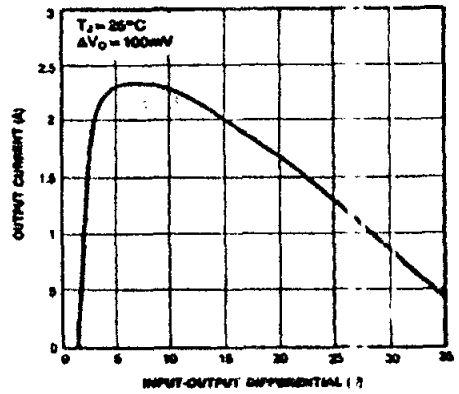


Figure 2. Peak Output Current

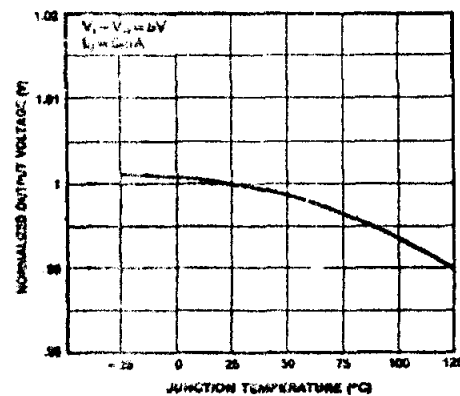


Figure 3. Output Voltage

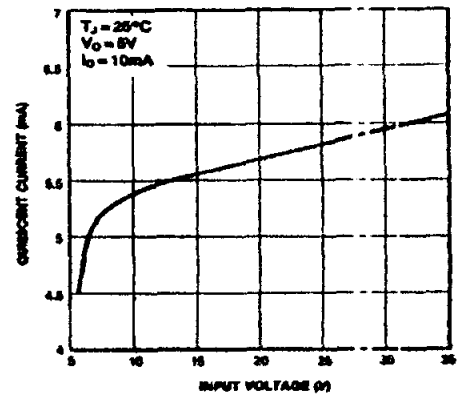


Figure 4. Quiescent Current

Typical Applications

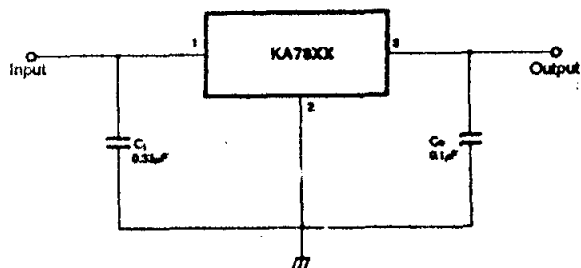


Figure 5. DC Parameters

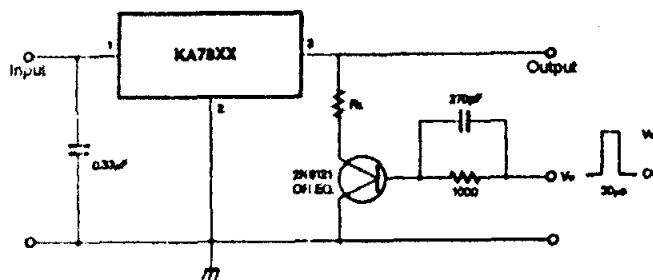


Figure 6. Load Regulation

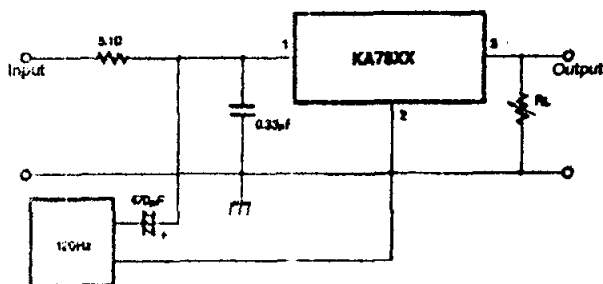


Figure 7. Ripple Rejection

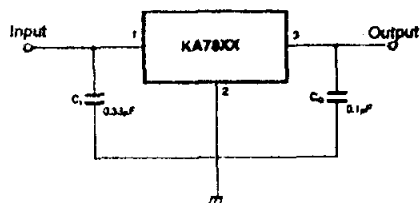


Figure 8. Fixed Output Regulator

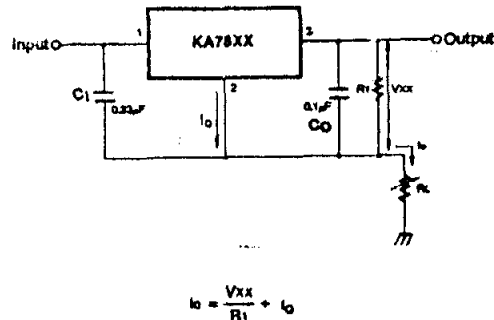
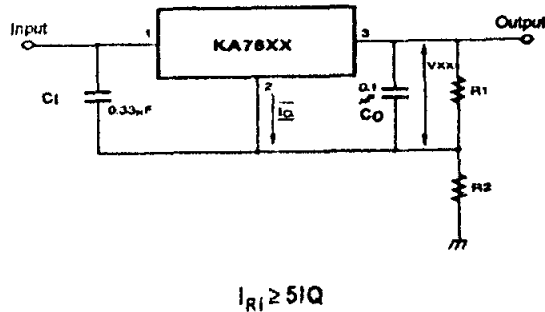


Figure 9. Constant Current Regulator

Notes:

- (1) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
- (2) C1 is required if regulator is located an appreciable distance from power Supply filter.
- (3) C0 improves stability and transient response.



$$V_O = V_{XX}(1 + R_2/R_1) + I_Q R_2$$

Figure 10. Circuit for Increasing Output Voltage

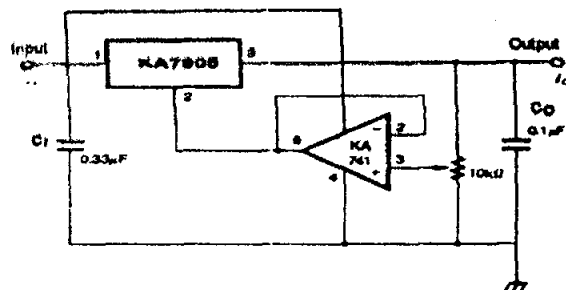


Figure 11. Adjustable Output Regulator (7 to 30V)

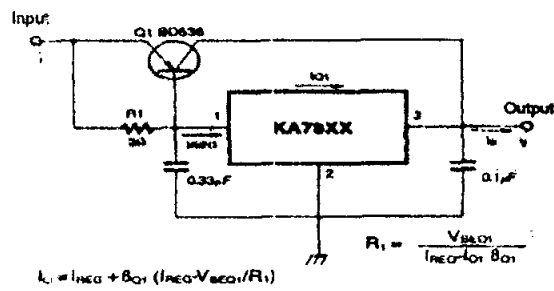


Figure 12. High Current Voltage Regulator

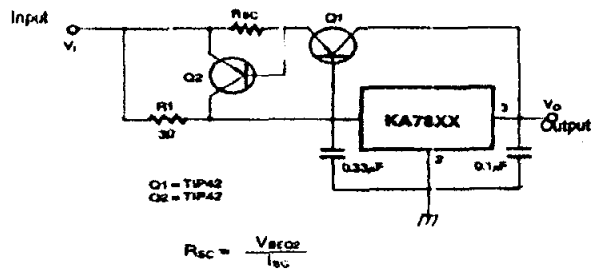


Figure 13. High Output Current with Short Circuit Protection

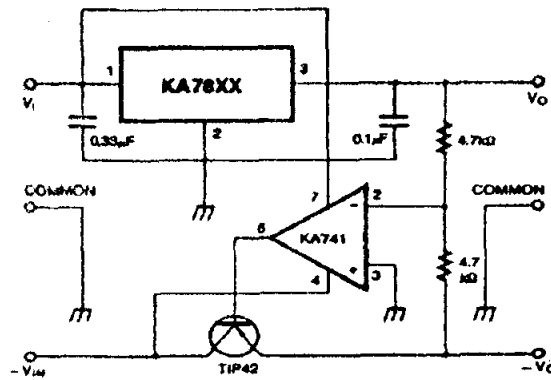


Figure 14. Tracking Voltage Regulator

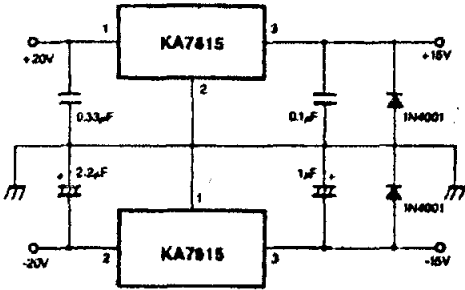


Figure 15. Split Power Supply (±15V-1A)

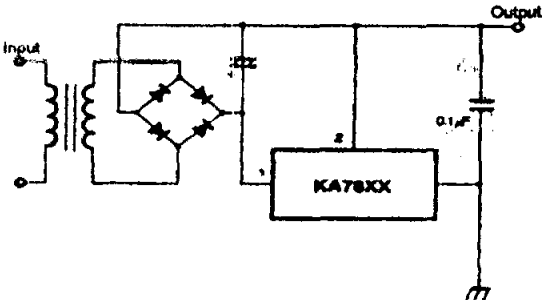


Figure 16. Negative Output Voltage Circuit

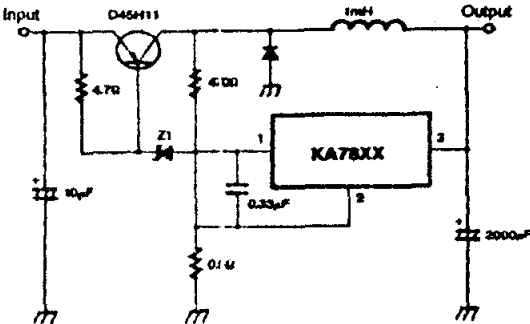
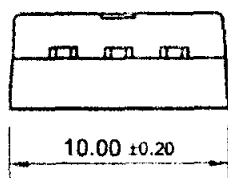
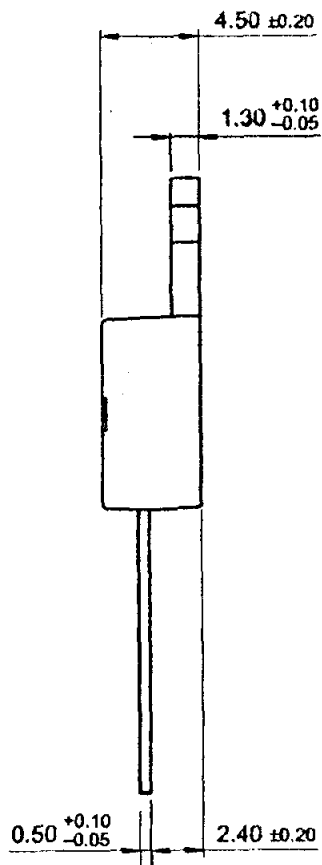
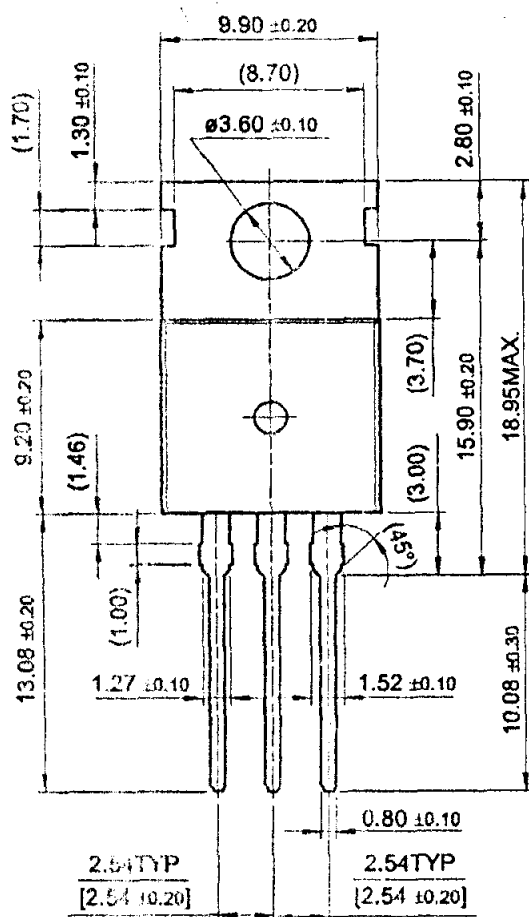


Figure 17. Switching Regulator

Mechanical Dimensions

Package

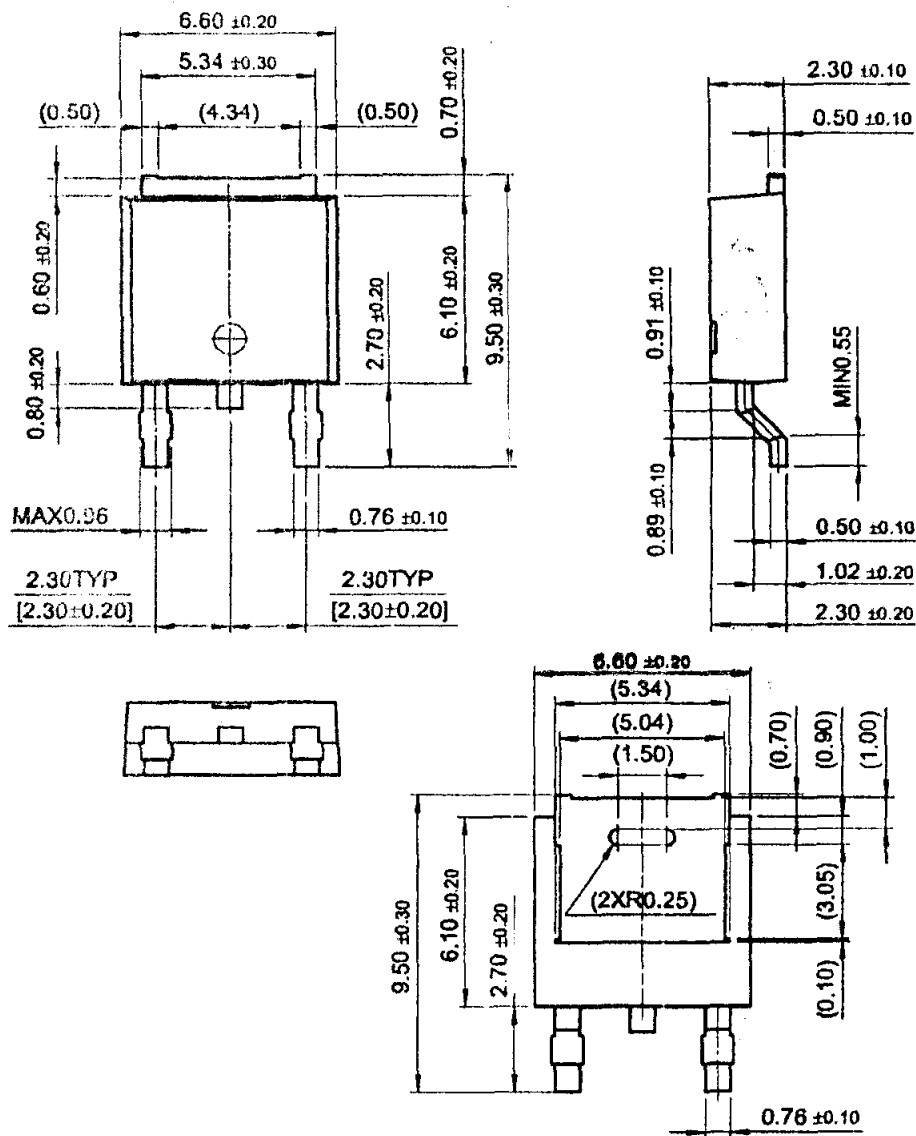
TO-220



Mechanical Dimensions (Continued)

Package

D-PAK



Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
KA7805 / KA7806	±4%	TO-220	0 ~ + 125°C
KA7808 / KA7809			
KA7810			
KA7812 / KA7815			
KA7818 / KA7824			
KA7805A / KA7806A	±2%		
KA7808A / KA7809A			
KA7810A / KA7812A			
KA7815A / KA7818A			
KA7824A			
KA7805R / KA7806R	±4%	D-PAK	
KA7808R / KA7809R			
KA7812R			

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

GP1A50HR/GP1A51HR GP1A52HR/GP1A53HR

OPIC Photointerrupter

■ Features

1. High sensing accuracy (Slit width : 0.5mm)
2. LSTTL and TTL compatible output
3. Both-side mounting type : GP1A50HR (Gap: 3mm)
Either-side mounting type : GP1A51HR (Gap: 3mm)
PWB mounting type : GP1A52HR (Gap: 3mm)
GP1A53HR (Gap: 5mm)

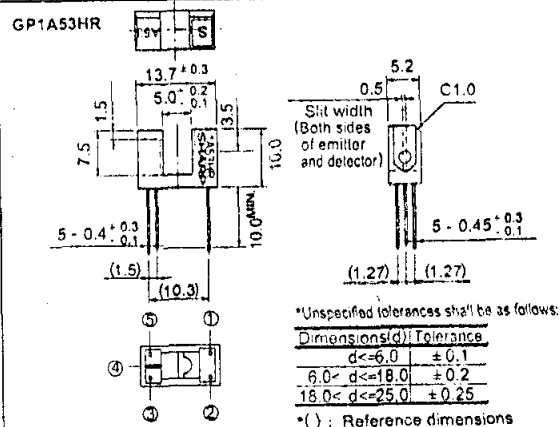
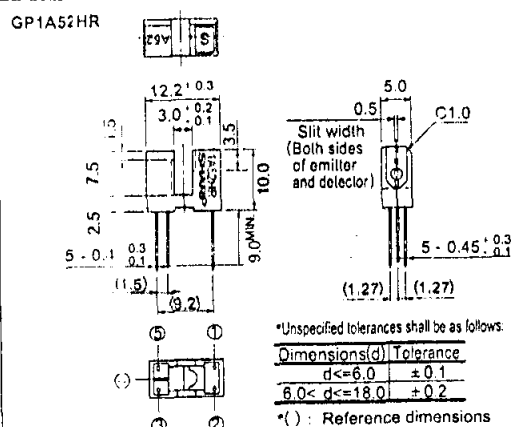
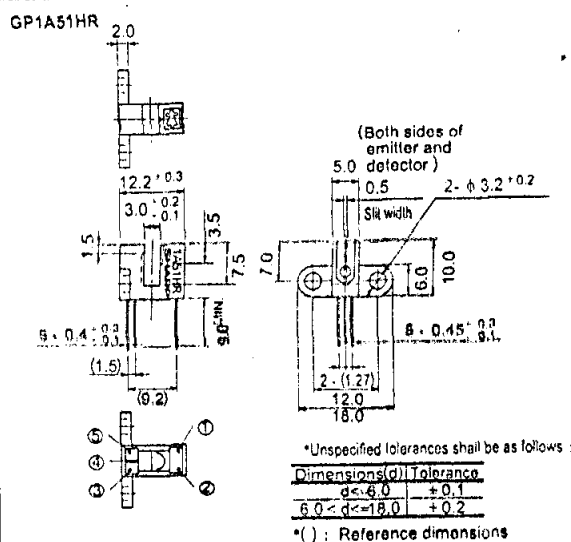
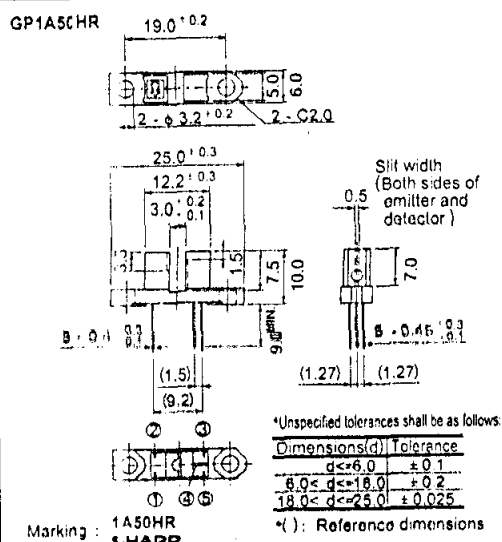
■ Applications

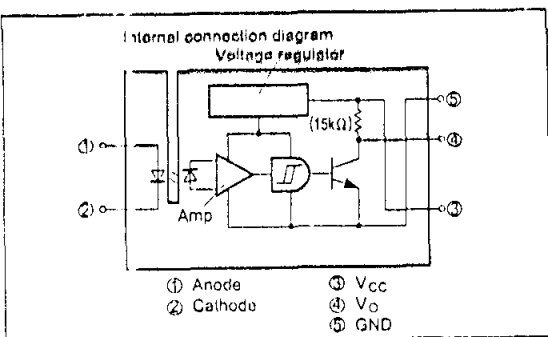
1. OA equipment, such as printers, facsimiles, etc.
2. VCRs

***"OPIC" (Optical IC) is a trademark of the SHARP Corporation.
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Outline Dimensions

(Unit : mm)





Absolute Maximum Ratings

(T_a = 25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I _F	50	mA
	*1 Peak forward current	I _{FM}	1	A
	Reverse voltage	V _R	6	V
	Power dissipation	P	75	mW
Output	Supply voltage	V _{CC}	- 0.5 to + 17	V
	Output current	I _O	50	mA
	Power dissipation	P _O	250	mW
Operating temperature		T _{opr}	- 25 to + 85	°C
Storage temperature		T _{stg}	- 40 to + 100	°C
*2 Soldering temperature		T _{sol}	260	°C

*1 Pulse width: 100 μs, Duty ratio: 0.01

*2 For 5 seconds

Electro-optical Characteristics

(T_a = 25°C)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage	GP1A50HR/GP1A51HR GP1A52HR	V _F I _F = 5mA	-	1.1	1.4	V
		GP1A53HR	V _I I _I = 8mA	-	1.14	1.4	V
	Reverse current	I _R	V _R = 5V	-	-	10.0	μA
Output	Operating supply voltage	V _{CC}		4.5	-	17.0	V
	Low level output voltage	V _{OL}	V _{CC} = 5V, I _F = 0, I _{OL} = 16mA	-	0.15	0.4	V
	High level output voltage	V _{OH}	V _{CC} = 5V, *1 I _F = 5mA	4.9	-	-	V
	Low level supply current	I _{CC1}	V _{CC} = 5V, I _F = 0	-	1.7	3.8	mA
	High level supply current	I _{CC2}	V _{CC} = 5V, *1 I _F = 5mA	-	0.7	2.2	mA
Transfer characteristics	"Low→High" threshold input current	GP1A50HR/GP1A51HR GP1A52HR	I _{TH1} V _{CC} = 5V	-	1.0	5.0	mA
		GP1A53HR	I _{TH2} V _{CC} = 5V	-	1.5	8.0	mA
	Hysteresis	I _{TH1} /I _{TH2}	V _{CC} = 5V	0.55	0.75	0.95	
	Propagation delay time	"Low→High" propagation delay time	V _{CC} = 5V, *1 I _F = 5mA R _L = 280Ω	-	3.0	9.0	μs
		"High→Low" propagation delay time		-	5.0	15.0	
		Rise time		-	0.1	0.5	
		Fall time		-	0.05	0.5	

*1 I_{TH1} represents forward current when output changes from low to high.*2 I_{TH2} represents forward current when output changes from high to low. Hysteresis stands for I_{TH1}/I_{TH2}.*3 GP1A53HR Condition of V_{OH}, I_{CC2}. Response time; I_F = 8mA

OPTO 22

DATA SHEET

SOLID-STATE RELAYS

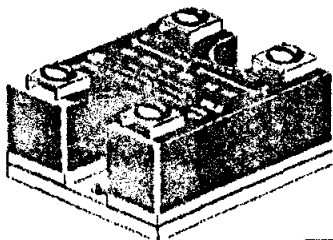
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Form 059-040726

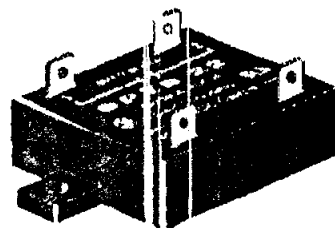
Overview

In 1974, Opto 22 introduced the first liquid epoxy-filled line of power solid-state relays (SSR). This innovation in SSR design greatly improved the reliability and reduced the cost of manufacturing. At that time, we also incorporated into our manufacturing process 100% testing of every relay produced under full load conditions. By 1978, Opto 22 had gained such a

reputation for reliability that we were recognized as the world's leading manufacturer of solid-state relays. Through continuous manufacturing improvements and the same 100% testing policy established 22 years ago, Opto 22 is still recognized today for the very high quality and reliability of its complete line of solid-state relays.



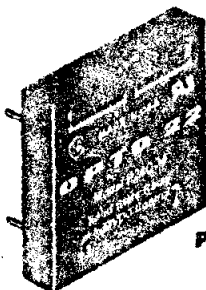
Power Series



Z Series

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P Series



MP Series

Opto 22 • 43044 Business Park Drive • Temecula, CA 92590 • Phone: (951) 695-3000 • (800) 321-OPTO • Fax: (951) 695-3085 • www.opto22.com

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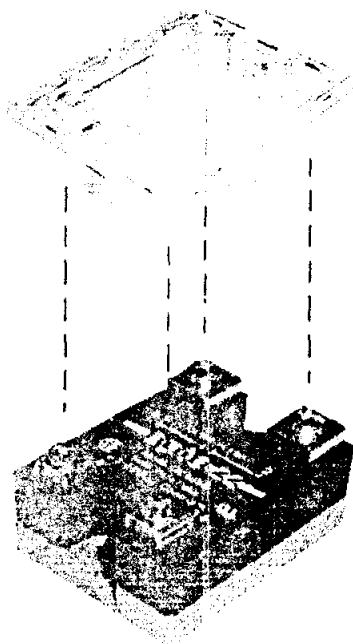
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Specifications

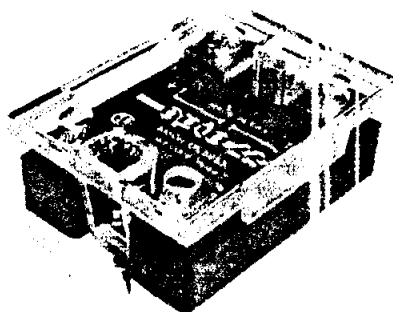
All Models

- 4,000 V optical isolation input to output
- Zero voltage turn-on
- Turn-on time: $\frac{1}{2}$ cycle maximum
- Turn-off time: $\frac{1}{2}$ cycle maximum
- Operating frequency: 25 to 65 Hz (operates at 400 Hz with six times off-state leakage)
- Coupling capacitance input to output: 8 pF maximum
- Hermetically sealed
- DV/DT Off-state: 200 volts per microsecond
- DV/DT commutating: snubbed for rated current at 0.5 power factor
- UL recognized
- CSA certified
- CE component
- See Opto 22 form #986 for torque specifications.

Safety Cover for Power Series SSRs



A plastic safety cover (Opto 22 part number: SAFETY COVER) is optionally available for Opto 22 Power Series SSRs. The safety cover reduces the chance of accidental contact with relay terminals, while providing access holes for test instrumentation.



Optional plastic safety cover installed on a Power Series SSR

OPTO 22

DATA SHEET

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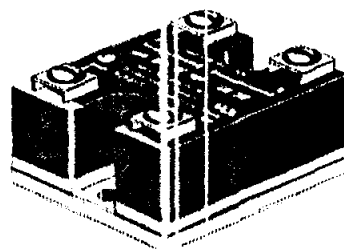
SOLID-STATE RELAYS

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Specifications

AC Power Series - 120/240 Volt

Opto 22 provides a full range of power series relays with a wide variety of voltage (110-575) and current options (3-45 amps). All Power Series relays feature 4,000 volts of optical isolation and have a high FRV rating.



Model Number	Nominal AC Line Voltage	Nominal Current Rating (Amps)	1 cycle Surge (Amps) Peak	Nominal Signal Input Resistance (Ohms)	Signal Pick-up Voltage	Signal Drop-out Voltage	Peak Repetitive Voltage Maximum	Maximum Output Voltage Drop	Off-State Leakage (mA) maximum	Operating Voltage Range (Volts AC)	PI Rating mW (ms)	Isolation Voltage	qjc* (°C/Watt)	Dissipation (Watts/Amp)
12003	120	3	85	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	2.5mA	12-140	30	4,000Vrms	11	1.7
120010	120	10	110	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	7 mA	12-140	50	4,000Vrms	1.3	1.6
120025	120	25	250	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	7 mA	12-140	250	4,000Vrms	1.2	1.3
120045	120	45	650	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	7 mA	12-140	1750	4,000Vrms	0.67	0.9
24003	240	3	85	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	5 mA	24-280	30	4,000Vrms	11	1.7
240010	240	10	110	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	14 mA	24-280	50	4,000Vrms	1.3	1.6
240025	240	25	250	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	14 mA	24-280	250	4,000Vrms	1.2	1.3
240045	240	45	650	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	14 mA	24-280	1750	4,000Vrms	0.67	0.9
380025	380	25	250	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	12 mA	24-420	250	4,000Vrms	1.2	1.3
380045	380	45	650	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	12 mA	24-420	1750	4,000Vrms	0.67	0.9
120A10	120	10	110	13K	85 VAC (280 allowed)	10 VAC	600	1.6 volts	7 mA	12-140	80	4,000Vrms	1.3	1.6
120A25	120	25	250	33K	85 VAC (280 allowed)	10 VAC	600	1.6 volts	7 mA	12-140	250	4,000Vrms	1.2	1.3
240A10	240	10	110	33K	85 VAC (280 allowed)	10 VAC	600	1.6 volts	14 mA	24-280	50	4,000Vrms	1.3	1.6
240A25	240	25	250	33K	85 VAC (280 allowed)	10 VAC	600	1.6 volts	14 mA	24-280	250	4,000Vrms	1.2	1.3
240A45	240	45	650	33K	85 VAC (280 allowed)	10 VAC	600	1.6 volts	14 mA	24-280	1750	4,000Vrms	0.67	0.9

Notes: qjc* = Thermal resistance junction to base. Maximum junction temperature is 110°C.

** Operating Frequency: 25 to 65 Hz (operates at 400 Hz with 6 times the offstate leakage)

OPTO 22

SOLID-STATE RELAYS

DATA SHEET

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Form 859-040726

Specifications:

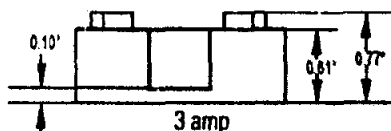
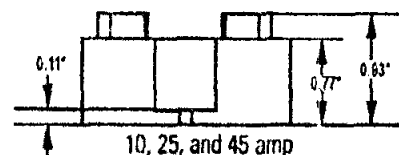
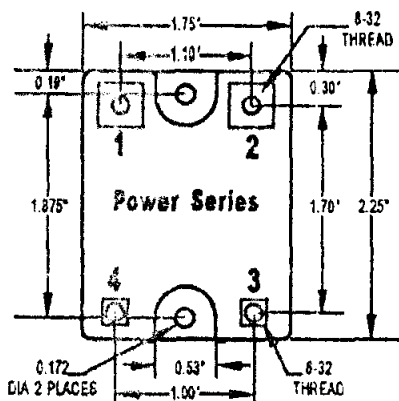
AC Power Series - 120/240 Volt (Continued)

Surge Current Data

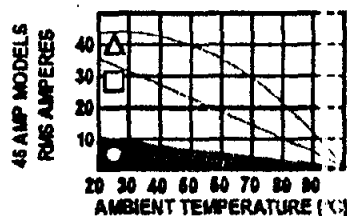
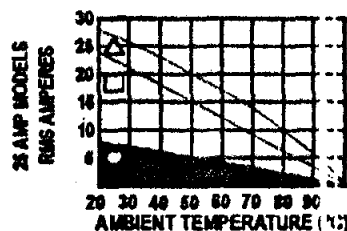
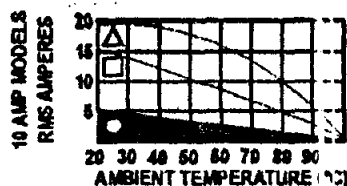
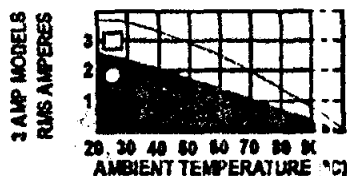
Time (Seconds)	Time (Cycles)	3-Amp Peak Amps	10-Amp Peak Amps	25-Amp Peak Amps	45-Amp Peak Amps
0.017	1	85	110	250	650
0.060	3	66	85	175	420
0.100	6	53	70	140	320
0.200	12	45	60	112	245
0.500	30	37	50	80	175
1	60	31	40	67	134
2	120	28	33	53	119
3	180	27	32	49	96
4	240	26	31	47	85
5	300	25	30	45	81
10	600	24	28	42	84

Note: *60 Hz.

Dimensional Drawings



Thermal Ratings



- FREE AIR
- MOUNTED ON 6\"/>

OPTO 22

SOLID-STATE RELAYS

DATA SHEET

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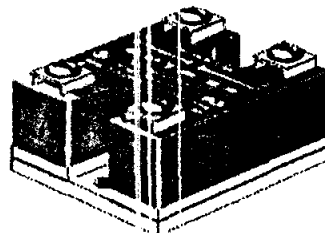
Form 850-040726

Specifications

AC Power Series - 480/575 Volt

DC SERIES: The DC Series delivers isolated DC control to large OEM customers worldwide.

AC SERIES: The AC Series offers the ultimate in solid-state reliability. All AC power series relays feature a built-in snubber and zero voltage turn-on. Transient proof models offer self-protection for noisy electrical environments.



Model Number	Nominal AC Line Voltage	Nominal Current Rating (Amps)	1 cycle Surge (Amps) Peak	Nominal Signal Input Resistance (Ohms)	Signal Pick-up Voltage	Signal Drop-out Voltage	Peak Repetitive Voltage Maximum	Maximum Output Voltage Drop	Off-State Leakage (mA) Maximum	Operating Voltage Range (Volts AC)	Pt. Rating (watts)	Isolation Voltage	θ_{JA} (°C/Watt)	Dissipation (Watts/Amps)
480D10-12	480	10	110	1000	3VDC (32V Allowed)	1 VDC	1200	3.2 volts	11 mA	100-630	50	4,000V rms	1.2	2.5
480D15-12	480	15	150	1000	3VDC (32V Allowed)	1 VDC	1200	3.2 volts	11 mA	100-630	50	4,000V rms	1.2	2.5
480D25-12	480	25	250	1000	3VDC (32V Allowed)	1 VDC	1000	1.8 volts	11 mA	100-630	250	4,000V rms	1.3	1.3
480D45-12	480	45	650	1000	3VDC (32V Allowed)	1 VDC	1000	1.8 volts	11 mA	100-630	1750	4,000V rms	0.67	0.9
575D15-12	575	15	150	1000	3VDC (32V Allowed)	1 VDC	1200	3.2 volts	15 mA	100-600	90	4,000V rms	1.2	2.5
575D45-12	575	45	650	1000	3VDC (32V Allowed)	1 VDC	1000	1.8 volts	15 mA	100-600	1750	4,000V rms	0.67	0.9

Note: θ_{JA} = Thermal resistance junction to base. Maximum junction temperature is 110°C.

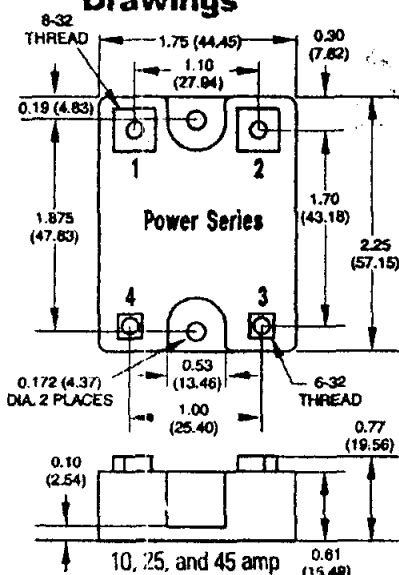
** Operating Frequency: 25 to 65 Hz (operates at 400 Hz with 6 times the off-state leakage)

Dimensional Drawings

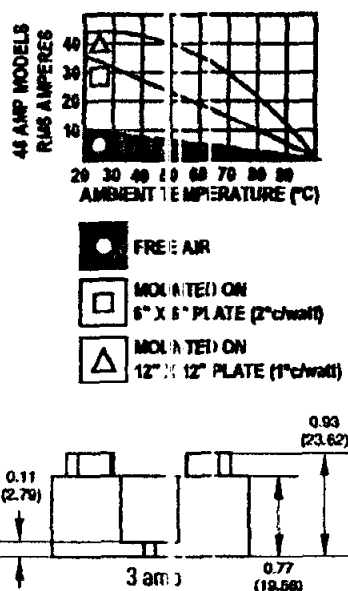
Surge Current Data

Time Second	Cycles	10-Amp Peak Amps	15-Amp Peak Amps	25-Amp Peak Amps	45-Amp Peak Amps
0.017	1	110	150	250	650
0.050	3	85	140	175	420
0.100	6	70	110	140	320
0.200	12	60	90	112	245
0.500	30	50	70	80	175
1	60	40	55	67	134
2	120	33	46	53	110
3	180	32	47	49	98
4	240	31	43	47	95
5	300	30	40	45	91
10	600	28	36	42	84

Note: ** 60 Hz



Thermal Ratings



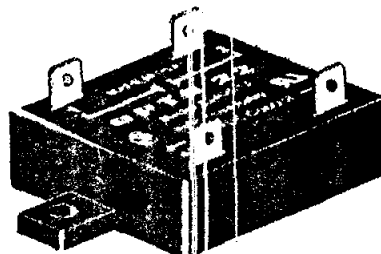
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Specifications

AC Power Series - 120/240 Volt Plastic Package (Z Series)

The Z Series employs a unique heat transfer system that makes it possible for Opto 22 to deliver a low-cost, 10-amp, solid-state relay in an all-plastic case. The push-on tool-free quick-connect terminals make the Z Series ideal for high-volume OEM applications.

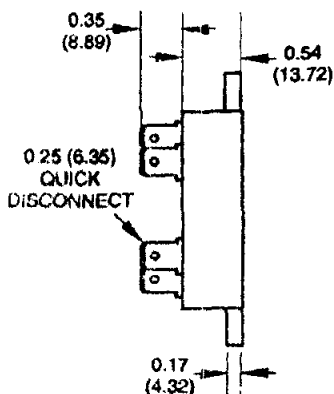
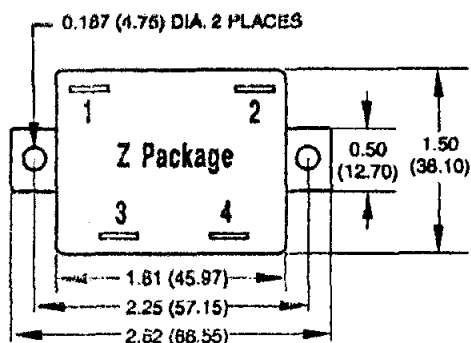


Model Number	Nominal AC Line Voltage	Nominal Current Rating (Amps)	1 cycle Surge (Amps) Peak	Nominal Signal Input Resistance (Ohms)	Signal Pickup Voltage	Signal Drop-out Voltage	Peak Repetitive Voltage Maximum	Maximum Output Voltage Drop	Off-State Leakage (mA) Maximum	Operating Voltage Range (Volts AC)	Pt Rating (Watts)	Isolation Voltage	θ_{JA}^* (°C/Watt)	Dissipation (Watt/Amp)
Z120D10	120	10	110	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	6 mA	12-140	50	4,000 Vrms	4	1
Z240D10	240	10	110	1000	3VDC (32V allowed)	1 VDC	600	1.6 volts	12 mA	24-280	50	4,000 Vrms	4	1

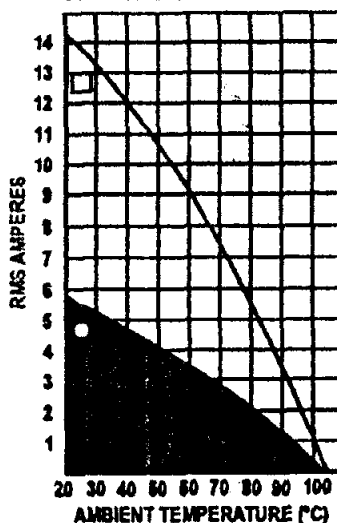
Notes: θ_{JA}^* = Thermal resistance junction to base. Maximum junction temperature is 110°C.

** Operating Frequency: 25 to 65 Hz (operates at 400 Hz with 5 times the off-state leakage)

Dimensional Drawings



Current vs. Ambient Ratings



Surge Current Data

Time Sec	Time Cycles	Peak Amps
0.01	1	110
0.01	3	85
0.1	6	70
0.2	12	60
0.5	30	50
1	60	40
2	120	33
3	180	32
4	240	31
5	300	30
10	600	28

Note: 60 Hz



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SOLID-STATE RELAYS

DATA SHEET

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Specifications

AC Power - Printed Circuit Package (P & MP Series)

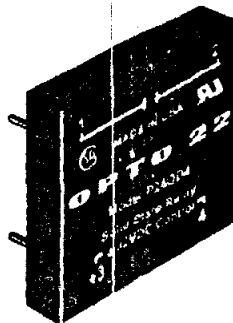
Model Number	Nominal AC Line Voltage	Nominal Current Rating (Amps)	1 cycle Surge (Amps) Peak	Nominal Signal Input Resistance (Ohms)	Signal Pick-up Voltage	Signal Drop-out Voltage	Peak Repetitive Voltage Maximum	Maximum Output Voltage Drop	On-State Leakage mA Maximum	Operating Voltage Range (Volts AC)	PI Rating (m.s.) (ms)	Isolation Voltage	θ_{JA} °C/Watt	Max Isolation Test Load
MP128D2 or P128D2	120	2	20	1000	3VDC*** (32V allowed)	1 VDC	600	1.5 volts	5 mA	12-140	2	4,000 Vrms	20	1.2
MP128D4 or P128D4	120	4	85	1000	3VDC*** (32V allowed)	1 VDC	600	1.5 volts	5 mA	12-140	30	4,000 Vrms	6.5	1.2
MP248D2 or P248D2	240	2	20	1000	3VDC*** (32V allowed)	1 VDC	600	1.5 volts	5 mA	24-280	2	4,000 Vrms	20	1.2
MP248D4 or P248D4	240	4	85	1000	3VDC*** (32V allowed)	1 VDC	600	1.5 volts	5 mA	24-280	30	4,000 Vrms	6.5	1.2
MP388D4	380	4	85	1000	3VDC*** (32V allowed)	1 VDC	800	1.5 volts	5 mA	24-430	30	4,000 Vrms	6.5	1.2

Notes: θ_{JA} = Thermal resistance junction to base. Maximum junction temperature is 110°C.
 oncy: 25 to 66 Hz (operates at 400 Hz with 8 times the offstate leakage)
 *** = MP Series 24 volts maximum.

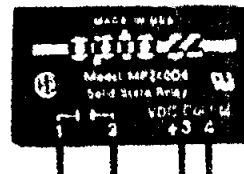
Surge Current Data

Time Second	Time* (Cycles)	Peak Amps	Peak Amps
0.017	1	20	85
0.050	3	18	66
0.100	6	15	53
0.200	12	11	46
0.500	30	9	37
1	60	8.5	31
2	120	8	28
3	180	7.5	27
4	240	7	26
5	300	6.5	25
10	600	6	24

Note: *60 Hz

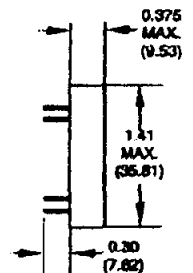
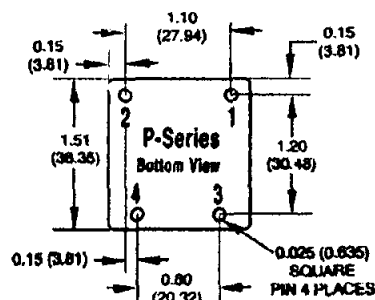
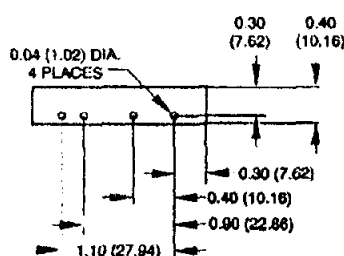
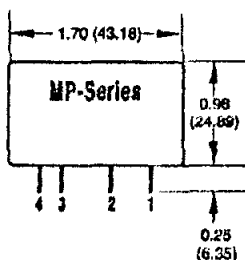


Model
P248D4



Model
MP128D4

Dimensional Drawings



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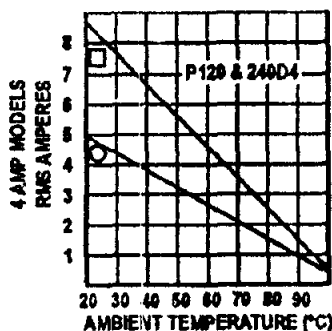
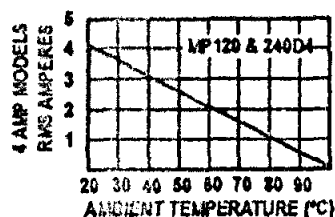
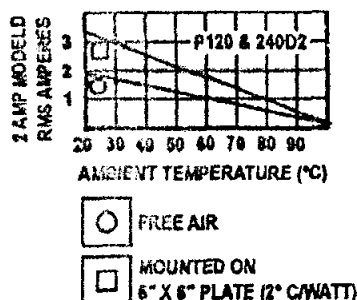
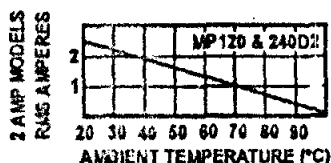
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Form 859-040726

Specifications

AC Power - Printed Circuit Package (P & MP Series)

Thermal Ratings



Surge Current Data

Time Second	Time* (Cycles)	Peak Amps	Peak Anips
0.017	1	20	85
0.050	3	18	66
0.100	6	15	53
0.200	12	11	45
0.500	30	9	37
1	60	8.5	31
2	120	8	28
3	180	7.5	27
4	240	7	25
5	300	6.5	25
10	600	6	24

Note: *60 Hz

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DATA SHEET

SOLID-STATE RELAYS

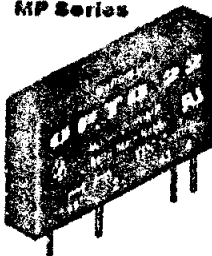
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Description

DC Switching Series

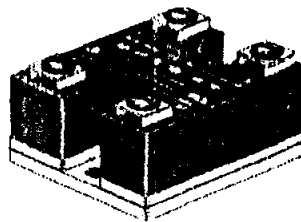
MP Series



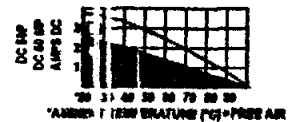
P Series



Power Series



Thermal Ratings



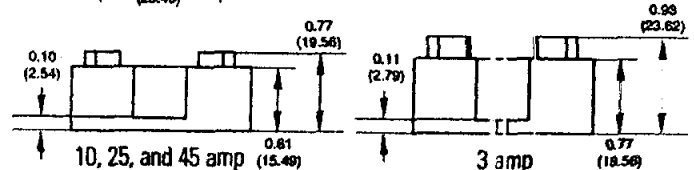
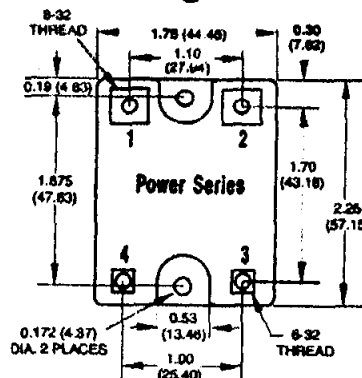
FREE AIR
2" C WATT HEAT SINK
(8" x 6" PLATE)

Specifications

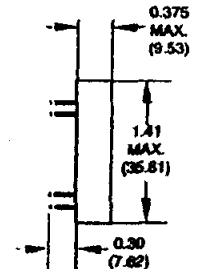
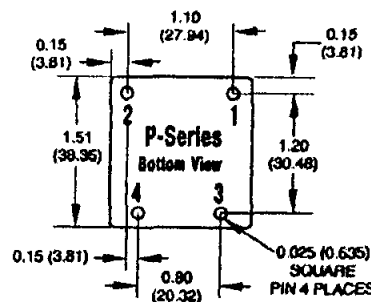
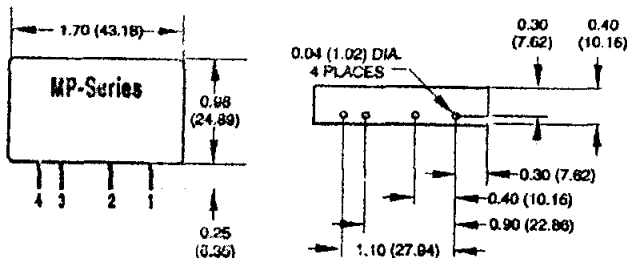
	DC60P or DC200P	DC60S-3	DC60S-5
Operating Voltage Range	5-60 VDC	5-60 VDC	5-60 VDC
Forward Voltage Drop	1.5 volts	1.5 volts at 1 amp	1.5 volts at 5 amps
Normal Current Rating	5 amps	1 amp	5 amps
Off-State Blocking	60 VDC	250 VDC	60 VDC
Signal Pickup Voltage	3 VDC 32 Volts* allowed	3 VDC 32 Volts* allowed	3 VDC 32 Volts* allowed
Signal Dropout Voltage	1 VDC	1 VDC	1 VDC
Signal Input Impedance	1,000 ohms	1,000 ohms	1,000 ohms
1 Second Surge	5 amps	2 amps	10 amps
Operating Temp. Range	-40° C to 100° C	-40° C to 100° C	-40° C to 100° C
Isolation Voltage	4,000 Vrms	4,000 Vrms	4,000 Vrms
Off-state Leakage	1 mA maximum	1 mA maximum	1 mA maximum
Package Type	P/M series	P series	Power series
Turn-On Time	100 µsec	100 µsec	100 µsec
Turn-Off Time	750 µsec	750 µsec	750 µsec

Note: *MP series maximum allowed control signal 24 VDC.

Dimensional Drawings



Dimensional Drawings



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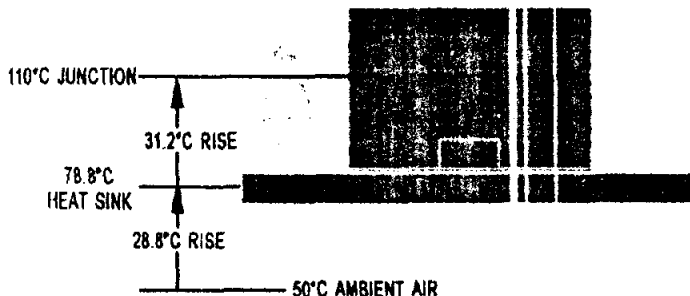
Applications

Tips

Heat Sink Calculation

Like all semiconductor devices, SSR current ratings must be based on maximum junction temperature. All Opto 22 SSRs operate conservatively at maximum junction temperatures of 110° C. Determining an adequate heat sink for a given SSR conducting a given current is very simple.

Note: Thermally conductive grease must be used between the relay base and the heat sink.



Sample Calculation Given:

120-Volt, 20-Amp Load
50° C Ambient Air

Choose Model 120D25 SSR.

Calculate dissipation as: **20 amps x 1.3 Watts per amp = 26 Watts**

Calculate temperature rise junction to SSR base as: **26 Watts x 1.2° C per Watt = 31.2° C**

Calculate allowable temperature of heat sink by subtracting 31.2° C from 110° C allowable junction temperature:

$$110^{\circ}\text{C} - 31.2 = 78.8^{\circ}\text{C}$$

The heat sink is in a 50°C ambient, therefore, allowable temperature rise on heat sink is: **78.8° C - 50° C = 28.8° C**

If heat sink is allowed to rise 28.8° C above ambient, then the thermal resistance of the heat sink is simply the 28.8° C rise divided by the 26 Watt. Any heat sink having a thermal resistance less than 1.1° C per Watt will be adequate.

Duty Cycle Calculation

When solid-state relays are operated in an on/off mode, it may be advantageous to calculate the RMS value of the current through the SSR for heat sinking or determining the proper current rating of the SSR for the given application.

I_{RMS} = RMS value of load or SSR

T_1 = Time current is on

T_2 = Time current is off

I_{ON} = RMS value of load current during on period

$$I_{\text{RMS}} = \sqrt{\frac{(I_{\text{ON}})^2 \times T_1}{T_1 + T_2}}$$

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Applications

Tips (Continued)

Transformer Loads

Careful consideration should be given to the selection of the proper SSR for driving a given transformer. Transformers are driven from positive saturation of the iron core to negative saturation of the core each 1/2 cycle of the alternating voltage. Large inrush currents can occur during the first 1/2 cycle of line voltage when a zero voltage SSR happens to turn on during the positive 1/2 cycle of voltage when the core is already in positive saturation. Inrush currents greater than 10 times rated transformer current can easily occur. The following table provides a guide for selecting the proper SSR for a given transformer rating.

120-Volt Transformers	
SSR MODEL	TRANSFORMER
P or MP 120D2	100 VA
Z120D10	500 VA
120D3	100 VA
P or MP 120D4	250 VA
120D10 or 120A10	500 VA
120D25 or 120A25	1 KVA
120D45	2 KVA
240-Volt Transformers	
P or MP240D2	200 VA
7240D10	1 KVA
120D3	200 VA
P or MP240D4	500 VA
240D10 or 240A10	1 KVA
240D25 or 240A25	2 KVA
240D45	4 KVA
480-Volt Transformers	
SSR MODEL	TRANSFORMER
480D10-12	5-Amp Primary
480D15-12	5-Amp Primary

Solenoid Valve and Contactor Loads

All Opto 22 SSRs are designed to drive inductive loads such as solenoid valves and electromechanical contactors. The built-in snubber in each SSR assures proper operation into inductive loads. The following table is a guide in selecting an SSR to drive a solenoid or contactor.

120-Volt Coils		
SSR CURRENT RATING	SOLENOID	CONTACTOR
2-Amp	1-Amp	NEMA Size 4
4-Amp	3-Amp	NEMA Size 7
240-Volt Coils		
SSR CURRENT RATING	SOLENOID	CONTACTOR
2-Amp	1-Amp	NEMA Size 7
4-Amp	3-Amp	NEMA Size 7

Control Current Calculation

All Opto 22 DC controlled SSRs have a control circuit consisting of 1000 ohms in series with an LED. Since 3 volts is required to turn on any SSR, the maximum current required is (3 volt - 1 volt) divided by 1000 ohms which equals 20 mA. The 1 volt is subtracted from the 3 volt signal because 1 volt is dropped across the LED. For higher control voltages, an external resistor can be added in series with the control voltage to limit the control current. To limit the control current to 2 mA, calculate the external resistor $R_c = 500 (E_c - 3)$ where E_c = the control voltage.

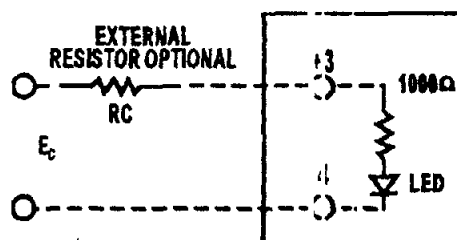
The DC control voltage range is 3-32 VDC. To calculate the control current for any voltage within the 3-32 VDC range, use the formula:

$$I_c = \frac{E_c - 1}{1000}$$

where R_c = zero.

With a 5V control signal,

$$I_c = \frac{5 - 1}{1000} = 4 \text{ mA}$$



Applications

Tips (Continued)

Opto 22 SSRs for controlling single-phase motors are shown in the following tables:

120-Volt Single-Phase Non-Reversing Motors	
SSR Model	MOTOR RATING
P or MP120D2	1 Amp
Z120D10	1/4 HP
120D3	1-1/2 Amp
P or MP120D4	1-1/2 Amp
120D10 or 120A10	1/4 HP
120D25 or 120A25	1/3 HP
120D45	3/4 HP

240-Volt Single Phase Non-Reversing Motors	
SSR Model	MOTOR RATING
P or MP240D2	1 Amp
Z240D10	1/4 HP
240D3	1-1/2 Amp
P or MP240D4	1-1/2 Amp
240D10 or 240A10	1/3 HP
240D25 or 120A25	1/2 HP
240D45	1-1/2 HP

120-Volt Single-Phase Reversing Motors	
SSR Model	MOTOR RATING
P or MP240D2	1 Amp
Z240D10	1/4 HP
240D3	1-1/2 Amp
P or MP240D4	1-1/2 Amp
240D10 or 240A10	1/4 HP
240D25 or 120A25	1/3 HP
240D45	3/4 HP

240-Volt Single-Phase Reversing Motors	
SSR Model	MOTOR RATING
480D10-12	1/4 HP
480D15-12	1/4 HP

Solid-State Relays In Series

In applications requiring greater current rating at higher voltage, two Opto 22 SSRs may be operated in series for double the voltage rating. The built-in snubber in each SSR assures proper voltage sharing of the two SSRs in series. In the diagram below, two 240-volt, 45-amp SSRs are connected in series for operation on a 480-volt line. The control is shown with a parallel hook-up but it should be noted that a serial connection can also be implemented.

Applications

Tips (Continued)

Lamp Loads

Since all Opto 22 SSRs are zero voltage switching, they are ideal for driving incandescent lamps because the initial inrush current into a cold filament is reduced. The life of the lamp is increased when switched by a zero voltage turn on SSR. The following table is a guide to selecting an Opto 22 SSR for switching a given incandescent lamp.

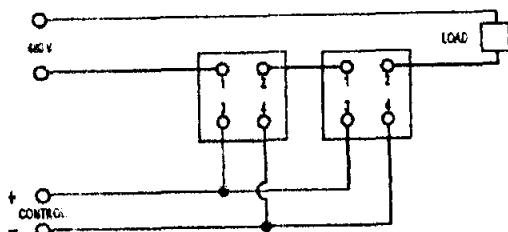
120 Volt Lamps	
SSR CURRENT RATING	LAMP RATING
2-Amp	100 Watt
4-Amp	400 Watt
10-Amp	1 Kilowatt
25-Amp	2 Kilowatt
45-Amp	3 Kilowatt
240 Volt Rating	
SSR CURRENT RATING	LAMP RATING
2-Amp	200 Watt
4-Amp	800 Watt
10-Amp	2 Kilowatt
25-Amp	4 Kilowatt
45-Amp	6 Kilowatt

Heater Loads

Care should be taken in selecting a SSR for driving a heater load if the load is cycled on and off in a continuous manner as might occur in a temperature control application. Constant cycling can cause thermal fatigue in the thyristor chip at the point where the chip bonds to the lead frame. Opto 22 employs a thick copper lead frame for mounting the SCR chips in the power series SSRs to eliminate thermal fatigue failures. In addition, Opto 22 recommends operating any SSR at 75% rated current for cycling heater loads to ensure complete reliability.

The following table is a guide to selecting the proper SSR for a given heater load.

Nominal SSR Current Rating	Maximum Recommended Heater Current
2-Amp	1½-Amp
4-Amp	2½-Amp
10-Amp	7½-Amp
25-Amp	18-Amp
45-Amp	35-Amp
10 480V	8-Amp
10 480V	8-Amp



Form 859-040726

Applications

Tips (Continued)

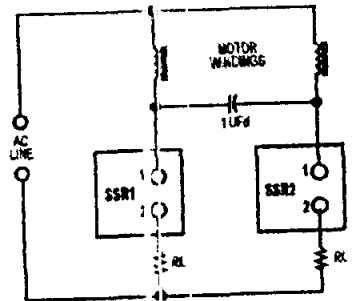
Single-Phase Reversing Motor Control

The circuit diagram illustrates a typical 1 Ø motor winding inductance and the phase shift capacitor can cause twice line voltage to appear across the open SSR. A 240-volt SSR should be used for a 120-Volt line. During the transition period when one SSR is turned on and the other SSR is going off, both SSRs may be on. In this case, the capacitor may discharge through the two SSRs, causing large currents to flow, which may destroy the SSRs. The addition of RL as shown will protect the SSRs from the short circuit capacitor discharge current.

$$\text{CALCULATE RL as: } RL = \frac{1.4 \text{ EAC}}{10 \times \text{SSR full load rating}}$$

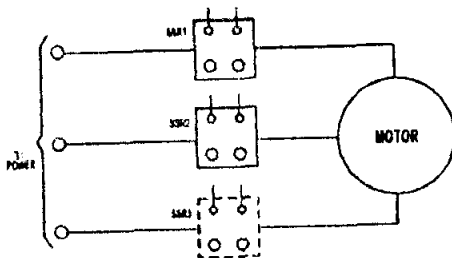
EXAMPLE: 10 amp SSR
120 V AC Line

$$RL = \frac{1.4 \times 120}{10 \times 10} = 1.7 \text{ ohm}$$



The resistors are unnecessary if the control circuit is designed to ensure one SSR is off before the other SSR is on.

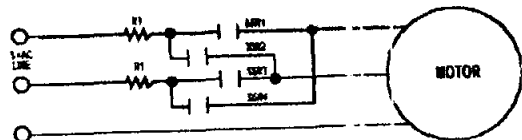
Three-Phase Motor Control



Three-phase motors may be controlled by solid-state relays as shown. A third SSR as shown is optional, but not necessary. The control windings may be connected in series or parallel. Care should be taken to ensure that surge current drawn by the motor does not exceed surge current rating of the SSR.

240-Volt 3ø Motors	
SSR MODEL	MOTOR
Z240D25	1/3 HP
Z240D10	3/4 HP
240D10	3/4 HP
240A10	3/4 HP
240D25	2 HP
240A25	2 HP
240D45	3 HP
480-Volt 3ø Motors	
SSR MODEL	MOTOR
480D10-12	1-1/2 HP
480D15-12	1-1/2 HP

Three-Phase Reversing Motor Control



Three-phase reversing motor control can be implemented with four SSRs as shown in the connection diagram. The SSRs work in pairs with SSR1 and SSR3 operated for rotation in one direction and SSR2 and SSR4 operated for rotation in the reverse direction. The resistor R1 as shown in the connection diagram protects against line-to-line shorts if SSR1 and SSR4 or SSR3 and SSR2 are on at the same time during the reversing transition period. Use the following table as a guide to the proper selection of an SSR for this application.

Opto 22 Relay	Motor Full Load Rating	Resistor for 120V line	Resistor for 240V line
3-Amp	1.25-Amp	4 ohm 50 W	8 ohm 50 W
10-Amp	5-Amp	1 ohm 100 W	2 ohm 100 W
25-Amp	8-Amp	.5 ohm 100 W	1 ohm 100 W
45-Amp	16-Amp	.25 ohm 150 W	.5 ohm 150 W
15-Amp	5-Amp	1 ohm 100 W	2 ohm 100 W

FAQ

SSR Applications

Q: What is a solid-state relay?

A: A solid-state relay (SSR) is a semiconductor device that can be used in place of a mechanical relay to switch electricity to a load in many applications. Solid-state relays are purely electronic, normally composed of a low current "control" side (equivalent to the coil on an electromechanical relay) and a high-current load side (equivalent to the contact on a conventional relay). SSRs typically also feature electrical isolation to several thousand volts between the control and load sides. Because of this isolation, the load side of the relay is actually powered by the switched line; both line voltage and a load (not to mention a control signal) must be present for the relay to operate.

Q: What are the advantages of using an SSR over a mechanical relay?

A: There are many applications that require a moderate amount of power (W to kW) to be switched on and off fairly rapidly. A good example of this would be the operation of a heater element in a controlled-temperature system. Typically, the amount of heat put into the system will be regulated using pulse-width modulation turning a fixed-power heating element on and off for time periods ranging from seconds to minutes. Mechanical relays have a finite cycle life, as their components tend to wear out over thousands to millions of cycles. SSRs do not have this problem; in the proper application, they could be operated almost infinitely.

Q: What are the limitations of using an SSR?

A: SSRs have a few limitations when compared to the capabilities of their mechanical counterparts. First, because the relay is semiconductor-based, it will never turn all the way on, nor off. This means that in the "on" state, the relay still has some internal resistance to the flow of electricity, causing it to get hot. When in the "off" state, the relay will exhibit a small

Note: This is the SSR portion of the overall FAQ on the Opto 22 Web site. The entire FAQ can be found at: <http://www.opto22.com/support/faq/22ocsuppFaq.aspx>

amount of leakage current, typically a few μ A. This leakage can conspire to keep some loads, especially ones with a high impedance, from turning off! Additionally, SSRs are more sensitive to voltage transients; while Opto 22 relays are very well transient-protected, if a relay gets hit hard enough a sufficient number of times, it will die or degrade. This makes SSRs less ideal for driving highly inductive electromechanical loads, such as some solenoids or motors. SSRs should also never be used for applications such as safety power disconnects because even in the off state, leakage current is present. Leakage current through an SSR also implies the presence of a potentially high voltage. Even though the relay is not conducting a large amount of current, the switched terminal will still be "hot," and thus dangerous.

Q: Do you make multi-pole or multi-throw SSRs?

A: Opto 22 manufactures only single-pole, single-throw SSRs. If multi-phase operation is required, just use a relay on each phase. Because of the limitations on semiconductor devices of the type used in SSRs, it is not practical to build single-device multi-throw SSRs. However, an alternative to multi-throw operation may be accomplished with multiple relays.

Q: Can I hook up SSRs in parallel to achieve a higher current rating?

A: No. There is no way to guarantee that two or more relays will turn on simultaneously when operated in parallel. Each relay requires a minimum voltage across the output terminals to function; because of the optical isolation feature, the "contact" part of the SSR is actually powered by the line it switches. One relay turning on before the other will cause the second relay to lose its turn-on voltage, and it won't even turn on, or at least not until the first relay fails from carrying too much current.

FAQ (continued)

Q: What does a "zero-crossing" turn-on circuit refer to?

A: "Zero-crossing" turn-on and turn-off refer to the point on the AC wave form when the voltage is zero. It is at this point that an AC SSR will turn on or off. All Opto 22 AC relays are designed with a zero-crossing turn-on and turn-off circuit. When the AC circuit voltage is at zero, no current is flowing. This makes it much easier and safer for the semiconductor device in the relay to be turned on or off. It also generates much less electrical EMI/RFI noise.

Q: Can I use an AC SSR to switch DC?

A: No. Because of the zero crossing circuit described above, the relay will most likely never turn on, and even if it is on, it will likely not be able to be turned off, as DC voltage typically never drops to zero.

Q: Can I use a DC SSR to switch AC?

A: No. The semiconductor device used in Opto 22's DC SSRs is polarized. It may break down and conduct for the portion of the waveform that is reversed in polarity.

Q: Can a DC SSR be used to switch an analog signal?

A: This is not recommended at all, for several reasons. First, the voltage drop across the relay will cause signal loss. Second, the conduction characteristics of the SSR are very non-linear at low operating voltages and currents. Use a mechanical relay; it will work much better.

Q: What agency approvals do your SSRs carry?

A: In general, Opto 22 relays carry UL, CSA, and CE approval. See <http://www.opto22.com/support/agency.aspx>. Additionally, some SSRs contain VDE-approved optocouplers; contact Opto 22 for more information.

SSR Troubleshooting

Q: My SSR does not function anymore. What may have happened?

A: There is no "normal" mode of failure for SSRs. Most of the time, they just stop working, by refusing to turn on or off. Often, an improper installation is to blame for an SSR failure, as these are very simple, reliable devices. If you have a failed SSR, it is important to look at the normal operating parameters of that relay within the larger system to make sure that the relay being used is appropriate to the application, and that the relay is being properly installed in the system. The three most common causes of SSR failure are as follows:

- 1) SSR improperly matched to load.** The relay was destroyed by overheating from carrying too much current too long.
- 2) SSR insufficiently protected.** Remember, a semiconductor is less tough than a simple metal contact. Reverse voltages exceeding the PRV rating of the relay will cause damage. Voltage spikes on the switched line, perhaps from inductive kickback, destroyed one or more of the internal switching devices. Remember to use snubbers, transorbs, MOVs, and/or commutating diodes on highly inductive loads.
- 3) SSR improperly installed.** The SSR was not mounted to a large enough heat sink, or no thermal compound was used, causing the relay to overheat. Also, insufficient tightening of the load terminals can cause arcing and chronic heating of the relay. Opto 22 recommends 15 to 16 inch-pounds of torque on the load screw terminals. Similar failures have also been attributed to the use of crimp-on terminal lugs or spades; make sure such terminals are tightly crimped, and even drip some solder into the joint to ensure good electrical contact and protection from corrosion.

FAQ (continued)

Q: How can I test my SSR?

A: It is not possible to test an SSR by the same methods used to test mechanical relays; a typical SSR will always show an infinite impedance to a resistance meter placed across the output terminals. There are a few reasons for this. First, the SSR requires a small amount of power to operate, derived from whatever voltage source is placed on the load terminals. A typical multimeter will not supply sufficient voltage to cause the relay to change state. Second, AC SSRs contain a zero-crossing circuit, which will not allow them to change state unless zero voltage is applied. Most test equipment will supply a DC voltage to the relay, and the relay will thus never see the zero it requires to change state. To test an SSR, it is best to operate it at the actual line voltage it will be used at, driving a load such as a large light bulb.

Q: I have an SSR driving a load. The load turns on okay, but never seems to turn off, unless I remove power from the relay entirely. What might be happening?

A: This is normally a problem when using an SSR with a high-impedance load, such as a neon lamp or a small solenoid. Loads like these often have relatively large initial currents, but relatively small "hold in" currents. The result is that the off-state leakage current through the relay (see previous section) is insufficient to cause the load to turn on to start with, but sufficient to keep it on, once started. The solution to this is to place a power resistor, sized for 8–10 times the rated maximum leakage current for the SSR in parallel with the load. Make sure that this resistor has a high enough power rating for the application! For example, for a 5 mA leakage current at 120 VAC, a resistor drawing 50 mA would be desirable. Using Ohm's law, the resistor value becomes 2,400 Ohms. This resistor will dissipate 6 Watts, so a 7.5 or 10-Watt size power resistor should be used.

Q: I have a new AC SSR driving a solenoid. It turns on okay once, but will not turn on again. What is going on?

A: Some solenoids, some types of halogen lights, and some types of strobe lights incorporate a diode in series with the coil or filament. This causes the light to behave as a half-wave rectifier. Opto 22 SSRs have a built-in R-C snubber circuit in parallel with the output. The capacitor in this circuit charges up, but cannot discharge through the series diode, causing a voltage to appear across the SSR terminals. Because the SSR must see a zero voltage across the terminals to come on, it can't turn on again in this situation. The solution here would be to put a high-value resistor (several tens of Kohms) across the terminals of the relay, to allow the capacitor to drain its charge.

Products

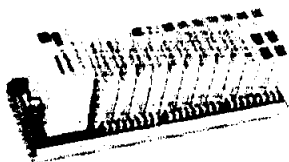
Opto 22 produces a broad array of reliable, flexible hardware and software products for industrial automation, remote monitoring, enterprise data acquisition, and machine-to-machine (M2M) applications.

Ethernet Systems

Based on the Internet Protocol (IP), SNAP Ethernet systems offer flexibility in their network connectivity and in the software applications they work with. The physical network may be a wired Ethernet network, a wireless network, or a modem. A wide variety of software applications can exchange data with SNAP Ethernet systems, including: Opto 22's own io² project™ suite of control and HMI software, manufacturing resource planning (MRP), enterprise management, and other enterprise systems. Human-machine interfaces (HMIs) and databases.

Mail systems: PC client software, custom applications, Modbus/TCP software and hardware.

SNAP Ethernet system hardware consists of controllers and I/O units. Controllers provide central control and data distribution. I/O units provide connection to sensors and equipment.



PLC OEM Systems

Opto 22 SNAP I/O systems are highly configurable, programmable controllers intended for OEMs, IT professionals, and others who need to develop custom software with Opto 22 SNAP I/O modules.

Linux® applications running on these systems can read and write to analog, simple digital, and serial I/O modules on SNAP I/O modules using easily implemented based operations. Applications can be developed using several common development tools and environments, including C or C++, Java, and shell scripts.



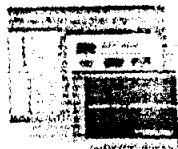
M2M Systems

Machine-to-machine (M2M) systems connect your business computer systems to the machines, devices, and environments you want to monitor, control, or collect data from. M2M systems often use wireless cellular communications to link remote facilities to central systems over the Internet, providing monitoring and control capability via a cellular phone.

Opto 22's Nvivo™ systems include everything you need for M2M—interface and communications hardware, data service plan, and Web interface—in one easy-to-use package. Visit nvio.opto22.com for more information.

Opto 22 Software

Opto 22's ioProject and FactoryFloor® software suites provide full-featured and cost-effective control, HMI, and OPC software to power your Opto 22 hardware. These software applications help you develop control automation solutions, build easy-to-use operator interfaces, and expand your manufacturing system's connectivity.



Quality

In delivering hardware and software solutions for worldwide device management and control, Opto 22 retains the highest commitment to quality. We do no statistical testing; each product is made in the U.S.A. and is tested twice before leaving our 160,000 square-foot manufacturing facility in Temecula, California. That's why we can guarantee solid-state relays and optically-isolated I/O modules for life.

Product Support

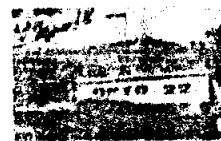
Opto 22's Product Support Group offers comprehensive technical support for Opto 22 products. The staff of support engineers represents years of training and experience, and can assist with a variety of project implementation questions. Product support is available in English and Spanish from Monday through Friday, 7 a.m. to 5 p.m. PST.

Opto 22 Web Sites

- www.opto22.com
- nvio.opto22.com
- www.internetio.com (live Internet I/O demo)

Other Resources

- OptoInfo CDs
- Custom integration and development
- Hands-on customer training classes.



About Opto 22

Opto 22 manufactures and develops hardware and software products for industrial automation, remote monitoring, enterprise data acquisition, and machine-to-machine (M2M) applications. Using standard, commercially available Internet, networking, and computer technologies, Opto 22's input/output and control systems allow customers to monitor, control, and acquire data from all of the mechanical, electrical, and electronic assets that are key to their business operations. Opto 22's products and services support automation end users, OEMs, and information technology and operations personnel.

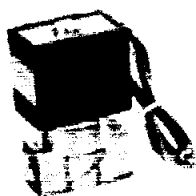
Founded in 1974 and with over 80 million Opto 22-connected devices deployed worldwide, the company has an established reputation for quality and reliability.

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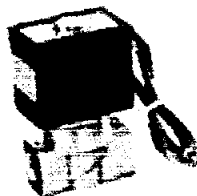
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—= UZ Series Solenoid Valve =—



● UZ-A-06



● UZ-A-08



● UZ-B-06, 08, 10



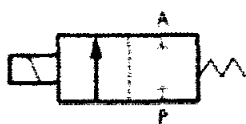
● UZ-C-06, 08, 10

■ Graphics Sign

● UZ-A-06, 08

● UZ-B-06, 08, 10

● UZ-C-06, 08, 10



• Ordering Code

UZ	A	06	H	AC220V
UZ 系列	结构类型 (Structure Type):	接管口径 (Pipe Size):	空白: 普通型 (Normal Type)	标准电压 (Standard Voltage):
	A/B: 二位二通 (2 Position 2 Ports)	06: G1/8	H: 高温型 (High- Temperature Type)	AC110V
	C: 二位三通 (2 Position 3 Ports)	08: G1/4		AC220V
		10: G3/8		AC380V
				DC24V

■ Specific Property

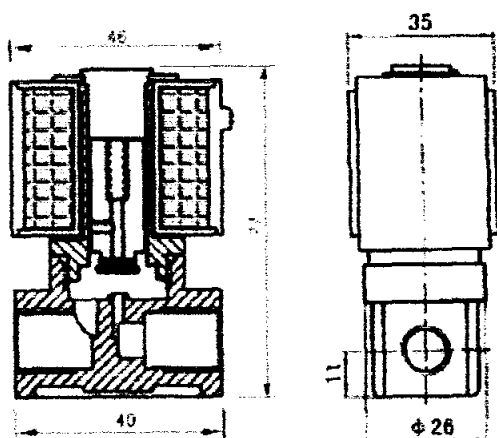
This valve has direct action type piston and quick action, with multiple purposes, high efficiency, long service life, good waterproof performance, multiple wiring directions and handsome shape.

■ Technical Parameter

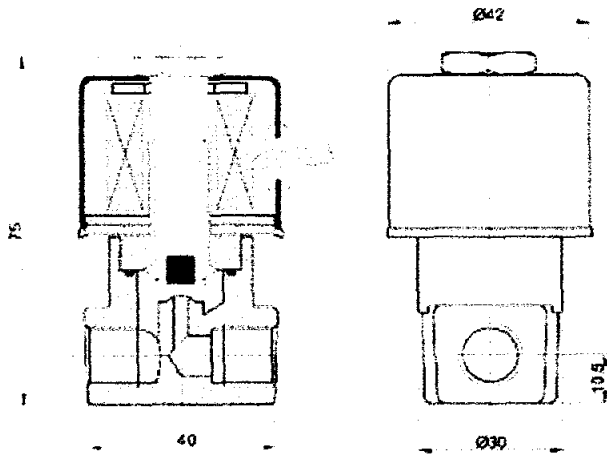
Material of Body	Brass				
Operating Method	Direct Action Type				
Pipe Size	G1/8	G1/4	G1/8	G1/4	G3/8
Nominal Diameter(mm)	2.5	2.5	4	5	6
Applicable Fluid	Air, Water, Oil(5CST below), Steam				
Pressure Range)	0~1.0MPa				
Applicable Temperature	Normal Type: -5~99°C High-Temperature Type: -5~185°C				
Specified Voltage	AC12V, AC24V, AC36V, AC110V, AC220V, AC380V, DC12V, DC24V, DC110V				
Operating Voltage Range	± 15%				
Min. Activating Time	0.05S				

■ Figure Dimension

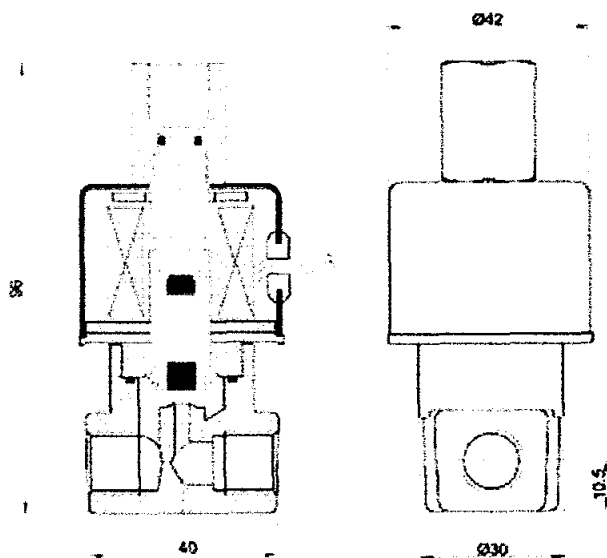
● UZ-A-06、08



● UZ-B-06, 08, 10



● UZ-C-06, 08, 10



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SURABAYA